

JEDEC STANDARD

DDR4 NVDIMM-P Bus Protocol

JESD304-4.01

(Minor editorial revision of JESD304-4, October 2020)

JANUARY 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DDR4 NVDIMM-P BUS PROTOCOL

(From JEDEC Board Ballot, JCB-20-26 and JCB-20-25, formulated under the cognizance of the JC-45.6 Subcommittee on Hybrid Modules.)

1. Scope

An NVDIMM-P device is defined as a LRDIMM memory module which provides host controller access to DRAM and/or other memory devices such as persistent memory. In order to enable access to media that may have non-deterministic access latencies, and/or on-board media management activities, which may temporarily delay access to non-volatile memory media, a handshake protocol is required to inform the host controller of availability/unavailability of return data from the DIMM. To mitigate the performance impact of this non-determinism, capabilities to enable out-of-order data transactions and to stack commands for enhanced data bus utilization are also required. A transactional protocol is described herein for NVDIMM-P, which may be used on a DDR interface allowing operation of both standard DRAM modules and NVDIMM-P modules on the same channel.

NVDIMM-P modules follow the DDR4 LRDIMM specification in pinout, electrical topology and behavior except as noted in this specification.

Minimal changes to the host controller can enable these technologies while allowing flexibility to optimize memory system performance. Options to simplify the protocol or implementation (at the expense of performance) are provided.

1.1 Reference Material

This NVDIMM-P protocol spec is a companion to the JEDEC DDR4 DRAM Standard, *JESD79-4B*, as well as the JEDEC DDR4 RCD/DB Standard and JEDEC DDR4 LRDIMM Common Standard.

2. Architecture and Initialization

2.1 NVDIMM-P bus architecture

Figure 1a shows an NVDIMM-P bus architecture example.

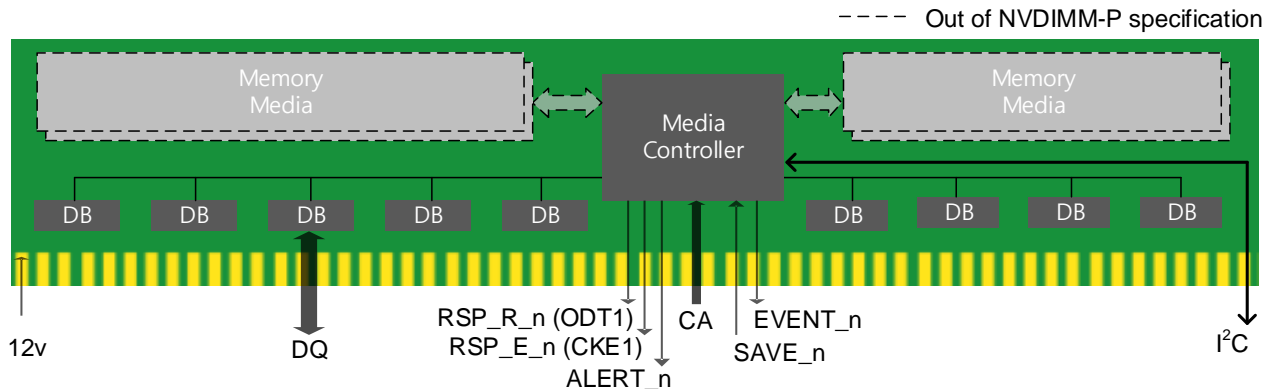


Figure 1a — Example of NVDIMM-P bus architecture

2.1.1 CA and Data bus

The command, address, and data pins of DDR4 NVDIMM-P are identical to DDR4 LRDIMM. Refer to the “JEDEC DDR4 LRDIMM Design Specification”.

2.1.2 Response Signal

Response signals are used to notify the data ready, event or error conditions described below.

- **RSP_R_n:** Response READY signal. Asynchronous, active-LOW, pulse-width modulated signal from NVDIMM-P to host indicating transactional/handshake signals such as when a read data packet is available, or when a status or error condition exists. One signal pin per NVDIMM-P is provided and directly connected to host.
- **RSP_E_n:** Response EXTRA signal. Asynchronous, active-LOW, pulse-width modulated signal from NVDIMM-P to host indicating persistent write completion. One signal pin per NVDIMM-P is provided and directly connected to host.
- **ALERT_n:** Response ERROR signal. Asynchronous, active-LOW, pulse-width modulated signal from NVDIMM-P to host indicating CA parity error and Write Channel error. One signal pin per NVDIMM-P is provided and shared with other SDRAM LRDIMM or NVDIMM in same channel to host.

To make the NVDIMM-P pin-out compatible with DDR4 LRDIMM, response signals are repurposed from existing DDR4 LRDIMM pins. Table 1 shows the pin assignments. Note that the ODT1 is repurposed for RSP_R_n and CKE1 is repurposed for RSP_E_n. Each NVDIMM-P has one (1) RSP_R_n signal and one (1) RSP_E_n signal. The pin assignment of the response signals is described in Table 1, “ - Response Signal Pin Assignment”.

Table 1 - Response Signal Pin Assignment

DDR4 LRDIMM			DDR4 NVDIMM-P		
Name	Pin number	Tx/Rx	Name	Pin number	Tx/Rx
ODT1	91	Rx	RSP_R_n	91	Tx
CKE1	203	Rx	RSP_E_n	203	Tx
ALERT_n	208	Tx	ALERT_n	208	Tx

The electrical characteristics of the response signal, RSP_R_n and RSP_E_n, shall follow the single ended AC & DC output levels and single-ended AC & DC input/output levels for DQ signals, respectively, as defined in the DDR4 SDRAM Specification, JESD79-4B. The electrical characteristics of ALERT_n are identical to DDR4 SDRAM ALERT_n. The response signal shall transmit asynchronously in order to convey read data, status or error message availability, via the use of pulse-width modulation to discern between response conditions. The encoding for the possible responses transmitted on the response signal is described in Table 2.

2.1.2 Response Signal (cont'd)

Table 2 - Response Signal Encoding

Response Signal	Response Pulse Width ^{1,2}	Symbol	Function	Description
RSP_R_n	2	RD_RDY	Read Ready	Read data or Message packet is available in buffers for host retrieval
	4	URGENT	Urgent Error	Urgent error detected on the bus or protocol. Host controller shall poll status immediately to respond to error condition or condition requiring additional action. See 7.1.6
RSP_E_n	2	W_PER	Write Persistency	Data has been written to NVM by flush request. See 4.5
	4	RFU	Reserved	Reserved for future use
ALERT_n	See Table 127	PAR_ERR	CA parity Error	CA parity Error is detected
	See Table 127	WECC_ERR	Write Channel Error	Write Channel error is detected

NOTE 1 Pulse width is in clock cycles (2UI). The response pulse is active LOW. The maximum response length is 8 UI, equivalent to a DQ burst length of 8. The maximum response pulse width is equivalent to 1.6Gbps @ DDR4-3200.

NOTE 2 Responses must be separated by a high pulse width of minimum tRSPH.

A RSP_R_n signal from the NVDIMM-P with a logic LOW pulse-width of two (2) clocks (4 UIs) indicates that message or requested data of XREAD is available in the DIMM output buffers.

The RSP_R_n signal with a logic LOW pulse-width of four (4) clocks (8UIs) conveys that an urgent error condition requiring immediate attention exists. A RSP_E_n signal from the NVDIMM-P with a logic LOW pulse-width of two (2) clocks (4UIs) conveys that a group of one or more data bursts has been committed to Non-Volatile Media (NVM).

A minimum tRSPH logic level HIGH time of two (2) clocks (4UIs) must be provided between any signaled responses. An example of pulse-width modulated signals on the RSP_R_n and RSP_E_n pin is described in the following figure.

The NVDIMM-P response signals are non-deterministic and independent. There is no timing correlation between the commands and the responses on each signal.

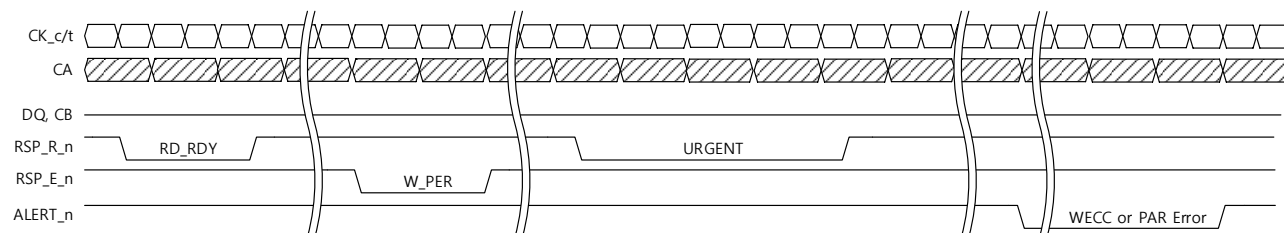


Figure 1b - Response Signaling

2.1.3 Event_n and Save_n

Event_n and Save_n pins are used for communication with the module management controller. See “Module Management Register” Specification for more details.

2.1.4 I2C bus

I2C bus is used to access SPD, MCW(Media controller Control Word) and MMR(Module Management Register). See 3.2 and “Module Management Register” Specification for more details.

2.2 Data packet format

For data read write operation, NVDIMM-P supports two different data packet formats:

- Option A: 4 user-defined metadata (user) bits and 3 write credit (WC) bits
- Option B: 6 user-defined metadata bits (user) and 1 Credit Threshold (CTH) bit

The data format is determined by the contents of MR2 A[13] bit during the power-up initialization. If MR2 A[13] bit is 0, Format A is used. If MR2 A[13] bit is 1, Format B is used.

Option A:

The NVDIMM-P returns packet information for each transaction containing of the following:

- 8 bits Read ID (RID)
- 1 bit data poison
- 4 bits user-defined metadata
- 3 bits Write Credit (WC)
- 48 bits Channel ECC

The transaction data packet format is described in the following tables.

Table 3 - Write data packet format for XWRITE and PWRITE

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Write Data0				Write Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RFU	RFU	RFU	RFU
CB7	POISON	RFU	RFU	RFU	RFU	RFU	RFU	RFU

Table 4 - Read data and message packet format for SEND

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Read Data0				Read Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RID[3]	RID[2]	RID[1]	RID[0]
CB7	POISON	WC[2]	WC[1]	WC[0]	RID[7]	RID[6]	RID[5]	RID[4]

NOTE RID≠FFh indicates read data packet, RID=FFh indicates message packet

Table 5 - Read data packet format for SREAD

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Read Data0				Read Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RFU	RFU	RFU	RFU
CB7	POISON	WC[2]	WC[1]	WC[0]	D_VALID	RFU	RFU	RFU

Option B:

The NVDIMM-P returns packet information for each transaction containing of the following:

- 8 bits Read ID (RID)
- 1 bit data poison
- 6 bits user-defined metadata
- 1 bits CTH(Credit Threshold)
- 48 bits Channel ECC

The transaction data packet format is described in the following tables. ,

Table 6 - Write data packet format for XWRITE and PWRITE

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Write Data0				Write Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RFU	RFU	RFU	RFU
CB7	POISON	RFU	USER	USER	RFU	RFU	RFU	RFU

Table 7 - Read data and message packet format for SEND

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Read Data0				Read Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RID[3]	RID[2]	RID[1]	RID[0]
CB7	POISON	CTH	USER	USER	RID[7]	RID[6]	RID[5]	RID[4]

NOTE RID≠FFh indicates read data packet, RID=FFh indicates message packet

Table 8 - Read data packet format for SREAD

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0~DQ63	Read Data0				Read Data1			
CB0~CB5	ECC				ECC			
CB6	USER	USER	USER	USER	RFU	RFU	RFU	RFU
CB7	POISON	CTH	USER	USER	D_VALID	RFU	RFU	RFU

2.2.1 Read ID

As part of the NVDIMM-P protocol, an explicit RID function is utilized whereby the host controller shall provide an 8-bit transaction Read ID (RID) value. By using the 8 bit RID, the NVDIMM-P supports up to 255 Out-of-Order read transactions. The NVDIMM-P will return the transaction RID along with transaction data as part of the transaction information bus.

2.2.2 Poison and User-defined metadata

Poison and User-defined metadata on writes is stored on NVDIMM-P and returned with corresponding data packet. In normal case, poison bit=1 is used to indicate the poisoned data by the host. Poison on writes is stored and returned as poisoned data on reads.

2.2.3 Data Valid (D_VALID)

This bit indicates the read data validity of a SREAD.

2.2.4 Write Credit (WC) and PWRITE Credit (PWC)

WC and PWC indicate available buffer space in NVDIMM-P at a 64-byte granularity. They are used to limit the number of outstanding XWRITE and PWRITE requests from the host. The total number of credits for XWRITE and PWRITE requests is defined in the message packet, which can be accessed with a READ_STATUS command on initialization. Refer to 2.3, “Message packet” and 4.6.2, “

Available Credit Synchronization” for details. The NVDIMM-P device provides write credit feedback to the host as part of the SEND or SREAD response packet using the WC [2:0] (option A) or CTH (option B) fields. The write credit from the NVDIMM-P indicates the number of released write credits (1 write credit represents a 64B write buffer space) since last write credit feedback.

Option A:

The poison bit represents the Poison case and differentiates between XWRITE and PWRITE write credit values as described below.

- Poison bit = 0 WC[2:0] are XWRITE credits, values defined in Table 9
- Poison bit = 1 and WC[2:0] = 000b Poison case, shown in Table 10
- Poison bit = 1 and WC[2:0] ≠ 000b WC[2:0] are PWRITE credits, values defined in Table 10

The poison bit is combined with the three WC[2:0] bits to encode write credits for 0 up to 64 credits. NVDIMM-P always returns the best encoding that is equal to or less than the actual number of credits to be returned.

Table 9 - Write Credit Return

POISION and WC value of SEND or SREAD packet				Returned Write Credit Value
POISON	WC[2]	WC[1]	WC[0]	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	4
0	1	0	0	8
0	1	0	1	16
0	1	1	0	32
0	1	1	1	64

Table 10 - Poison and PWRITE Credit return

POISION and WC value of SEND or SREAD packet				Returned PWRITE Credit or Poison
POISON	WC[2]	WC[1]	WC[0]	
1	0	0	0	Poison
1	0	0	1	1
1	0	1	0	2
1	0	1	1	4
1	1	0	0	8
1	1	0	1	16
1	1	1	0	32
1	1	1	1	64

Since Both WC and PWC are encoded over the same bits, only one of them can be returned with a given read data packet. The media controller should prioritize sending the credits back based on buffer demand for each.

Option B:

The Credit Threshold(CTH) bit represents a programmable write credit threshold value. This value is programmed by the host in mode register location MR2 A[2:0] using the same encoding as the Option A's scheme as shown in Table 9 and Table 10. When a new CTH value is programmed in MR2 A[2:0], the NVDIMM-P does not start using the new CTH value until it receives a READ_STATUS[01] (ADDR[3:2]=01b) command for the total available write buffer space. After the READ_STATUS command is received, the NVDIMM-P will return the three-bit CTH field in the READ_STATUS message packet and the change of incremental credit value will take effect.

If CTH = 0 in the read data or message packet metadata, then no credits are returned to the host. If CTH = 1 then credits based on the programmed value are returned to the host.

Poison bit is combined with CTH bits to return write credits as shown in below. The NVDIMM encodes the poison case with Poison=1 and CTH=0.

Table 11 - Credit Return with CTH

Poison	CTH	Comment
0	0	No Credits returned
0	1	WC returned
1	0	Poison Case
1	1	PWC returned

2.3 Message packet format

Table 12 defines the message packet delivered through the DQ bus. RID=FFh, POISON=0 and valid WC are delivered through CB6 and CB7 with the message packet. For any fields with multiple bits assigned for each DQ, the fields are transmitted from MSB to LSB of the field as the data beat increases from 0 to 7. There are two scenarios that the NVDIMM-P delivers the message packet to the host:

1) Initiated by media controller to deliver an internal event:

The NVDIMM-P generates a message packet and notifies it by asserting RD_RDY when the NVDIMM-P internal event occurs. After receiving a subsequent SEND command, the NVDIMM will transmit the message packet including the event information. The internal events are defined as follows:

- Internal Operation request (IOP)
- Interrupt (INT)
- Uncorrectable media Error (UE) of read request

Error RID return with POISON=1, VALID_ERR=1 and UE=1

2) Requested with a READ_STATUS command:

- A READ_STATUS command is received by the NVDIMM, requesting the NVDIMM-P to generate a message packet with status information. When the request is completed and the message packet is ready, the NVDIMM-P asserts the RD_RDY signal. After receiving a subsequent SEND command, the NVDIMM will transmit the STATUS information in a message packet. The message packet includes the following information. Refer to 4.6, “

Status register Read operation (**READ_STATUS**)” for more details.

- To request the completion of the power-up initialization (RDY_PWR)
When the internal initialization of NVDIMM-P controller is completed, a message packet with RDY_PWR=1 will be generated.
- To request the Available Write and PWRITE Credits
Message packet with Available Write and PWRITE Credits with VALID_WC=1 and VALID_PWC=1 will be generated.
- To request the RESET_RID (RDY_RID)
When all pending RID and output buffers for SEND command are cleared, a message packet with RDY_RID =1 will be generated.

Table 12 - NVDIMM-P Message Packet Format

	Name	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7	
DQ0	ERR_ALERT	VALID_ERR ^[1]	UE	RFU	RFU	RFU	RFU	RFU	RFU	
DQ1	RDY	RDY_PWR ^{[1][2]}	RFU	RFU	RFU	RDY_RID ^[3]	RFU	RFU	RFU	
DQ2	Available WC	VALID_WC ^[1]	User-defined CTH[2:0] ^[4]			Available WC[11:8]				
DQ3		Available WC [7:0]								
DQ4	IOP	VALID_IOP ^[1]	RFU	RFU	RFU		Mode	QoS[1:0]		
DQ5		RFU	IOP Time Shift[1:0]		IOP Time Unit[4:0]					
DQ6	Available PWC	VALID_PWC ^[1]	User-defined CTH[2:0] ^[4]			Available PWC[11:8]				
DQ7		Available PWC [7:0]								
DQ8	Available UNMAP_CNT	VALID_UNMAP ^[1]	RFU	RFU	RFU	Available UNMAP_CNT [11:8]				
DQ9		Available UNMAP_CNT[7:0]								
...								
DQ18	Interrupt	VALID_INT ^[1]	ADDR_VALID	RFU	RFU	INT_TYPE[3:0]				
DQ19		INT_STATUS[7:0]								
DQ20		INT_ADDR[7:0]								
DQ21		INT_ADDR[15:8]								
DQ22		INT_ADDR[23:16]								
DQ23		INT_ADDR[31:24]								
DQ24		INT_ADDR[39:32]								
...		...								
DQ63		ERID[7:0](Error RID) ^[5]								
CB0~CB5	ECC	ECC					ECC			
CB6	META ^[6]	RFU	RFU	RFU	RFU	1	1	1	1	
CB7		POISON	WC[2] / CTH	WC[1] / RFU	WC[0] / RFU	1	1	1	1	

NOTE 1 VALID_xxx (1-bit): Indicates whether the corresponding information is valid or not. 1: Valid, 0: Invalid. Once the valid corresponding information with VALID_xxx='1' is delivered through message packet, the VALID_xxx is automatically cleared at next message packet if there is no corresponding event.

NOTE 2 RDY_PWR (1-bit): Indicates the media controller ready after the completion of media controller initialization. Normal RDY_PWR value in message packet is '0'. After a READ_STATUS[00] command is received, only one message packet with RDY_PWR=1 is delivered when the initialization is completed.

NOTE 3 RDY_RID (1-bit): Indicates the XREAD/SREAD command ready after the completion of RESET-RID operation. Normal RDY_RID value in message packet is '0'. After a READ_STATUS[11] command is received, only one message packet with RDY_RID =1 is delivered when all prior read-requests and output buffer (for SEND command) are cleared.

NOTE 4 User-defined Programmable Write Credits (3bits): Host can change this value by setting MR2 A[2:0]. Same CTH value is used for WC and PWC.

NOTE 5 POISON, UE and ERID(Error RID) : POISON=1 indicates Uncorrectable media error is detected on the read requested address by XREAD/SREAD. The RID of XREAD/SREAD is reported by ERID bits. Once this event (POISON=1, VALID_ERR=1, UE=1) is delivered through the message packet, the POISON, VALID_ERR and UE bits are automatically cleared. See 7.1.4, "UE response of" for more details.

NOTE 6 Metadata order follows the order specified in F2RC4x DA[0]

3. Mode control and Status Register

The NVDIMM-P media controller includes both the DDR4 SDRAM Mode Register and DDR4 RCD Function space. Features supported in NVDIMM-P mirror the same DDR4 SDRAM MR and RCD address space. To support NVDIMM-P special functionality, several registers are added within this address space, which are defined in the following table.

Table 13 – NVDIMM-P special function registers

Register Name	Address
IOP mode0 enable/disable	MR1 A[6]
IOP mode1 enable/disable	MR1 A[5]
Interrupt enable/disable	MR1 A[17]
Credit Threshold	MR2 A[2:0]
Meta-data format(A or B)	MR2 A[13]
ECC enable/disable	MR3 A[13]
Advanced FIFO training mode enable/disable	MR6 A[8]
Internal media training start	MR6 A[9]
Training GuardKey enable/disable	MR6 A[13]
Media controller PLL/DLL locking status	MCW F2RC03-DA[0]
Media controller initialization status	MCW F2RC03-DA[1]
Meta-data ordering	MCW F2RC4x-DA[0]
tRRSE mode enable/disable	MCW F2RC4x-DA[1]
All-Zero Fail-Prevention enable/disable	MCW F2RC4x-DA[2]
Programmable READ(SEND) command delay	MCW F3RC00
Programmable WRITE command delay	MCW F3RC01

3.1 Mode Register

MR0

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	RFU	0 = must be programmed to 0 during MRS
A13, A11:9	WR	Write data Recovery time
A8	DLL Reset	0=NO, 1=YES
A7	TM	0=Normal, 1=Test
A12, A6,A5, A4, A2	CAS Latency (CL)	(See 3.1 Mode Register (cont'd) Table 15 ¹)
A3	Read Burst Type	0 = Sequential, 1 = Reserved
A1:A0	Burst Length	00 = 8 (Fixed) Abbreviated BL8MRS 01 = Reserved 10 = Reserved 11 = Reserved

NOTE 1 The table only shows the encodings for a given CAS Latency (CL). For actual supported CAS Latency, please refer to speed bin tables for each frequency.

Table 14 - Write data Recovery time (cycles)

A13	A11	A10	A9	Write recovery dealy
0	0	0	0	10
0	0	0	1	12
0	0	1	0	14
0	0	1	1	16
0	1	0	0	18
0	1	0	1	20
0	1	1	0	24
0	1	1	1	22
1	0	0	0	26
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	0

3.1 Mode Register (cont'd)

Table 15 - CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25
1	0	0	0	1	26
1	0	0	1	0	27
1	0	0	1	1	28
1	0	1	0	0	29
1	0	1	0	1	30
1	0	1	1	0	31
1	0	1	1	1	32
1	1	0	0	0	Reserved

3.1 Mode Register (cont'd)

MR1

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	Interrupt	0 = Disable, 1 = Enable
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff ¹	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable, 1 = Reserved
A10:8	RTT_NOM	000 = RTT_NOM Disable, other = Reserved
A7	Write Leveling Enable	0 = Disable, 1 = Enable
A6	IOP mode 0	0 = Disable, 1 = Enable
A5	IOP mode 1	0 = Disable, 1 = Enable
A4:3	Additive Latency	00 = 0(AL disabled), other = Reserved
A2:1	Output Driver Impedance Control	(See Table 16)
A0	DLL Enable	0 = Disable, 1 = Enable

NOTE Outputs disabled - DQs, DQS_ts, DQS_cs.

Table 16 - Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

3.1 Mode Register (cont'd)

MR2

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	RFU	0 = must be programmed to 0 during MRS
A13	Write Credit Update Option	0 = 3 bit 1 = 1 bit
A12	Write CRC	0 = Disable, 1 = Reserved
A11:9	RTT_WR	000 = Dynamic ODT Off, other = Reserved
A8	RFU	0 = must be programmed to 0 during MRS
A7:6	Reserved	0 = must be programmed to 0 during MRS
A5:3	CAS Write Latency (CWL) ^[1]	(See Table 17)
A2:0	Credit Threshold(CTH)	000 = reserved, 001 = 1, 010 = 2, 011 = 4 100 = 8, 101 = 16, 110 = 32, 111 = 64

NOTE CWL can be updated when MR6 A[13] (training guard key) is enabled.

Table 17 - CAS Write Latency (CWL)

A5	A4	A3	CWL	Speed Grade in MT/s for 1 tCK Write Preamble		Speed Grade in MT/s for 2 tCK Write Preamble	
				1 st Set	2 nd Set	1 st Set	2 nd Set
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	2933/3200	2400	2666	2400
1	1	0	18		2666	2933/3200	2666
1	1	1	20		2933/3200		2933/3200

NOTE The 2 tCK Write Preamble is valid for DDR4-2400/2666/3200 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional CWL is needed.

3.1 Mode Register (cont'd)

MR3

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	RFU	0 = must be programmed to 0 during MRS
A13	ECC disable	ECC disable mode in Normal mode 0 = ECC on, 1 : ECC off
A12:11	MPR Read Format	00 = Serial, 01 = Parallel, 10 = Staggered, 11 = Reserved
A10:9	Reserved	0 = must be programmed to 0 during MRS
A8:6	Reserved	0 = must be programmed to 0 during MRS
A5	Temperature sensor readout	0 = Disable, 1 = Reserved
A4	Per DRAM Addressability	0 = Disable, 1 = Reserved
A3	Reserved	0 = must be programmed to 0 during MRS
A2	MPR Operation	0 = Normal mode, 1 = Dataflow from/to MPR ^[1]
A1:0	MPR page Selection	00 = Page0, 10 = Page2, 01 = Page1, 11 = Page3 (See Table 17)

NOTE In MPR Mode Training, MPR training patterns are accessed through both ECC check bits and DQ bits. MPR data are accessed through both DQ and CB bus.

3.1 Mode Register (cont'd)

Table 18 - MPR Data Format with MPR page 0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00=MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01=MPR1	0	0	1	1	0	0	1	1	
	10=MPR2	0	0	0	0	1	1	1	1	
	11=MPR3	0	0	0	0	0	0	0	0	

Table 19 - MPR Data Format with MPR page 2 (MPR Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note	
BA1:BA0	00=MPR0	REVD	REVD	REVD	Temperature Sensor Status		Write CRC Enable	RTT_WR		Read-only	
		-	-	MR2	-	-	MR2	MR2			
		-	-	A11	-	-	A12	A10	A9		
	01=MPR1	REVD	REVD						REVD		
		MR6	MR6						MR3		
		A6	A5	A4	A3	A2	A1	A0	A3		
	10=MPR2	CAS Latency					CAS Write Latency				
		MR0					MR2				
		A6	A5	A4	A2	A12	A5	A4	A3		
	11=MPR3	RTT_NOM			RTT_PARK			Driver Impedance			
		MR1			MR5			MR1			
		A10	A9	A6	A8	A7	A6	A2	A1		

Table 20 - MPR Data Format with MPR page 3 (Vendor use only)¹

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00=MPR0	vendor	vendor	vendor	vendor	vendor	vendor	vendor	vendor	Read/Write
	01=MPR1	vendor	vendor	vendor	vendor	vendor	vendor	vendor	vendor	
	10=MPR2	vendor	vendor	vendor	vendor	vendor	vendor	vendor	vendor	
	11=MPR3	vendor	vendor	vendor	vendor	vendor	vendor	vendor	vendor	

NOTE MPR page3 is specifically assigned to NVDIMM-P. Actual encoding method is vendor specific.

3.1 Mode Register (cont'd)

MR4

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	RFU	0 = must be programmed to 0 during MRS
A13	Reserved	0 = must be programmed to 0 during MRS
A12	Write Preamble	0 = 1nCK, 1 = 2nCK
A11	Read Preamble	0 = 1nCK, 1 = 2nCK
A10	Read Preamble Training Mode	0 = Disable, 1 = Enable
A9	Reserved	0 = must be programmed to 0 during MRS
A8:6	CS to CMD/ADDR Latency Mode	000 = Disable, others = Reserved
A5	Reserved	0 = must be programmed to 0 during MRS
A4	Reserved	0 = must be programmed to 0 during MRS
A3	Reserved	0 = must be programmed to 0 during MRS
A2	Reserved	0 = must be programmed to 0 during MRS
A1	Reserved	0 = must be programmed to 0 during MRS
A0	Clock Stopped Power Down Mode	0 = Disable, 1 = Enable

MR5

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17:13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable, 1 = Reserved
A11	Write DBI	0 = Disable, 1 = Reserved
A10	Data Mask	0 = Disable, 1 = Reserved
A9	Reserved	Reserved
A8:6	RTT_PARK ^[1]	(See Table 21)
A5	ODT Input Buffer during Power Down Mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A4	Reserved	Reserved
A3	Reserved	Reserved
A2:0	Reserved	Reserved

NOTE RTT_PARK is defined for connections between the data buffer and the media controller.

3.1 Mode Register (cont'd)

Table 21 - RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

MR6

Address	Operation Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1,BA0	MR Select	000 = MR0, 001 = MR1, 010 = MR2, 011 = MR3, 100 = MR4, 101 = MR5, 110 = MR6, 111 = MR7
A17	RFU	0 = must be programmed to 0 during MRS
A13	Training Guard Key	0 = Disabled,1 = Enabled
A12:10	tDLLK	(See 3.1 Mode Register (cont'd) Table 22)
A9	Internal Training Media	0 = NOP(No Operation),1 = Start
A8	Advanced Training FIFO	0 = Disabled,1 = Enabled ²
A7	Reserved	0 = must be programmed to 0 during MRS
A6	Reserved	0 = must be programmed to 0 during MRS
A5:0	Reserved	0 = must be programmed to 0 during MRS

NOTE MR6 A[8](Advanced FIFO training) can be enabled when MR6 A[13] (training guard key) is enabled.

3.1 Mode Register (cont'd)

Table 22 - tDLLK

A12	A11	A10	tDLLKmin(nCK) ¹	Note
0	0	0	597	Data rate \leq 1333Mbps
0	0	1		1333Mbps < Data rate \leq 1866Mbps (1600/1866Mbps)
0	1	0	768	1866Mbps < Data rate \leq 2400Mbps (2133/2400Mbps)
0	1	1	1024	2400Mbps < Data rate \leq 2666Mbps (2666Mbps)
1	0	0		2666Mbps < Data rate \leq 3200Mbps (2933/3200Mbps)
1	0	1	RFU	
1	1	0		
1	1	1		

MR7

MR7 is used for the MCW(Media controller Control Word) and BCW(Buffer Control Word).

3.2 Media controller Control Word

The control words are programmed by the host controller using the MRS function with DBG1, DBG0, DBA1, DBA0 = 0111b.

The control word is clocked in when DCS0_n is LOW, DACT_n is HIGH and DA16/RAS_n, DA15/CAS_n, DA14/WE_n are LOW. Both the address of the control word and the settings are transmitted over DA[12:0].

The reset default state of all control words (except vendor specific ones) is '0'. Every time the device is reset, its default state is restored. Stopping the clocks (CK_t=CK_c=LOW) to put the device in low-power mode will not alter the control word settings.

Table 23 - Function Space 0

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F0RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				Reserved	
F0RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				Reserved	
F0RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				Timing and IBT	
F0RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				Reserved	
F0RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				Reserved	
F0RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Reserved	
F0RC06	0	0	0	0	0	0	1	1	0	setting[3:0]				Command Space and Controller Word definition	
F0RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved	
F0RC08	0	0	0	0	0	1	0	0	0	setting[3:0]				Reserved	
F0RC09	0	0	0	0	0	1	0	0	1	setting[3:0]				Power Saving Settings	
F0RC0A	0	0	0	0	0	1	0	1	0	setting[3:0]				NVDIMM Operating Speed	
F0RC0B	0	0	0	0	0	1	0	1	1	setting[3:0]				Operating Voltage VDD and VREF Source	
F0RC0C	0	0	0	0	0	1	1	0	0	setting[3:0]				Training	
F0RC0D	0	0	0	0	0	1	1	0	1	setting[3:0]				DIMM Configuration	
F0RC0E	0	0	0	0	0	1	1	1	0	setting[3:0]				Parity	
F0RC0F	0	0	0	0	0	1	1	1	1	setting[3:0]				Command Latency Adder	
F0RC1x	0	0	0	0	1	setting[7:0]					Internal Vref				
F0RC2x	0	0	0	1	0	setting[7:0]					I2C Bus				
F0RC3x	0	0	0	1	1	setting[7:0]					Fine Granularity NVDIMM Operating Speed				
F0RC4x	0	0	1	0	0	setting[7:0]					CW Source Selection				
F0RC5x	0	0	1	0	1	setting[7:0]					CW Destination Selection				
F0RC6x	0	0	1	1	0	setting[7:0]					CW Data				
F0RC7x	0	0	1	1	1	setting[7:0]					IBT				
F0RC8x	0	1	0	0	0	setting[7:0]					ODT				
F0RC9x	0	1	0	0	1	setting[7:0]					Reserved				
F0RCAx	0	1	0	1	0	setting[7:0]					Reserved				
F0RCBx	0	1	0	1	1	setting[7:0]					IBT and MRS Snoop				
F0RCCx ... F0RCFx	0	1	1	x	x	setting[7:0]					CA Parity Error Log				

NOTE 1 F0RC7x CA Input Bus Termination bits cover the following CA inputs : DA17, DC0, DC1, DC2

- NOTE 2 CKE power down mode is enabled
- NOTE 3 Context for operation training
- NOTE 4 Address mirroring for MRS commands is disabled.
- NOTE 5 DODT0 input buffer and IBT ON and passed to QxODT[0] output. DODT1 input buffer and IBT is OFF and QxODT1 output buffer is OFF. If RC8x DA5 is not set to '1', DODT0 is passed to BODT.

Table 24 - Function Space 1

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F1RC00.	0	0	0	0	0	0	0	0	0	setting[3:0]				Data Buffer Interface Driver Characteristics Control Word	
F1RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				Reserved	
F1RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				Reserved	
F1RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				Reserved	
F1RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				Reserved	
F1RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Data Buffer Interface Output Slew Rate	
F1RC06	0	0	0	0	0	0	1	1	0	setting[3:0]				Reserved for future use	
F1RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved for future use	
F1RC08 ... F1RC0F	0	0	0	0	0	1	x	x	x	setting[3:0]				Reserved for future use	
F1RC1x ... F1RC7x	0	x	x	x	x	setting[7:0]								Reserved	
F1RC8x	0	x	x	x	x	setting[7:0]								BCOM/BCKE/BODT Output Delay Control	
F1RC9x	0	x	x	x	x	setting[7:0]								BCK Output Delay Control	
F1RCAx ... F1RCFx	0	x	x	x	x	setting[7:0]								Reserved for future use	

Table 25 - Function Space 2

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F2RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				Reserved for future use	
F2RC01	0	0	0	0	0	0	0	0	0	1	setting[3:0]			Reserved for future use	
F2RC02	0	0	0	0	0	0	0	0	1	0	setting[3:0]			Reserved for future use	
F2RC03	0	0	0	0	0	0	0	0	1	1	setting[3:0]			NVDIMM-P controller status	
F2RC04	0	0	0	0	0	0	0	1	0	0	setting[3:0]			Reserved for future use	
F2RC05	0	0	0	0	0	0	0	1	0	1	setting[3:0]			Reserved for future use	
F2RC06	0	0	0	0	0	0	0	1	1	0	setting[3:0]			Reserved for future use	
F2RC07	0	0	0	0	0	0	0	1	1	1	setting[3:0]			Reserved for future use	
F2RC08 ... F2RC0F	0	0	0	0	0	1	x	x	x	x	setting[3:0]			Reserved for future use	
F2RC1x	0	0	0	0	1	setting[7:0]					Reserved for future use				
F0RC2x	0	0	0	1	0	setting[7:0]					Reserved for future use				
F0RC3x	0	0	0	1	1	setting[7:0]					NVDIMM-P controller status				
F2RC4x	0	0	1	0	0	setting[7:0]					Packet and timing option Control				
F2RC5x	0	0	1	0	1	setting[7:0]					Correctable Error Interrupt Threshold and Enable				
F2RC6x	0	0	1	1	0	setting[7:0]					Error Injection Mode				
F2RC7x	0	0	1	1	1	setting[7:0]					Error Address0/Mask0				
F2RC8x	0	1	0	0	0	setting[7:0]					Error Address1/Mask1				
F2RC9x	0	1	0	0	1	setting[7:0]					Error Address2/Mask2				
F2RCAx	0	1	0	1	0	setting[7:0]					Error Address3/Mask3				
F2RCBx	0	1	0	1	1	setting[7:0]					Error Address4/Mask4				
F2RCCx ... F2RCFx	0	1	1	x	x	setting[7:0]					Urgent Error Log				

Table 26 - Function Space 3

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F3RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				Programmable Read Command delay	
F3RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				Programmable Write Command delay	
F3RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				Reserved for future use	
F3RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				Reserved for future use	
F3RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				Reserved for future use	
F3RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Reserved for future use	
F3RC06	0	0	0	0	0	0	1	1	0	setting[3:0]				Reserved for future use	
F3RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved for future use	
F3RC08~F3RC09	0	0	0	0	0	1	0	0	x	setting[3:0]				VrefDQ0~3 Training	
F3RC0A~F3RC0B	0	0	0	0	0	1	0	1	x	setting[3:0]				VrefDQ4~7 Training	
F3RC0C~F3RC0D	0	0	0	0	0	1	1	0	x	setting[3:0]				VrefDQ8~11 Training	
F3RC0E~F3RC0F	0	0	0	0	0	1	1	1	x	setting[3:0]				VrefDQ12~15 Training	
F3RC1x	0	0	0	0	1	setting[7:0]								VrefDQ16~19 Training	
F3RC2x	0	0	0	1	0	setting[7:0]								VrefDQ20~23 Training	
F3RC3x	0	0	0	1	1	setting[7:0]								VrefDQ24~27 Training	
F3RC4x	0	0	1	0	0	setting[7:0]								VrefDQ28~31 Training	
F3RC5x	0	0	1	0	1	setting[7:0]								VrefDQ32~35 Training	
F3RC6x	0	0	1	1	0	setting[7:0]								VrefDQ36~39 Training	
F3RC7x	0	0	1	1	1	setting[7:0]								VrefDQ40~43 Training	
F3RC8x	0	1	0	0	0	setting[7:0]								VrefDQ44~47 Training	
F3RC9x	0	1	0	0	1	setting[7:0]								VrefDQ48~51 Training	
F3RCAx	0	1	0	1	0	setting[7:0]								VrefDQ52~55 Training	
F3RCBx	0	1	0	1	1	setting[7:0]								VrefDQ56~59 Training	
F3RCCx	0	1	1	0	0	setting[7:0]								VrefDQ60~63 Training	
F3RCDx	0	1	1	0	1	setting[7:0]								VrefDQ64~67 Training	
F3RCEx	0	1	1	1	0	setting[7:0]								VrefDQ68~72 Training	
F3RCFx	0	1	1	1	1	setting[7:0]								Reserved for future use	

Table 27 - Function Space 4

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F4RC8x~F4RCEx	0	0	0	0	0	1	x	x	x	setting[3:0]				Event Log	
F4RCFx	0	x	x	x	x	setting[7:0]								Reserved for future use	

Table 28 - Function Space 7

Control Word	Address Bit														Meaning
	12	11	10	09	08	07	06	05	04	03	02	01	00		
F7RC00~F7RC0F	0	0	0	0	0	x	x	x	x	setting[3:0]				Reserved for Future use	
F7RC1x	0	0	0	0	1	setting[7:0]					Data code Byte 02 Year Information				
F7RC2x	0	0	0	1	0	setting[7:0]					Data code Byte 12 Work Week Information				
F7RC3x	0	0	0	1	1	setting[7:0]					Data code Byte 22 Reserved				
F7RC4x	0	0	1	0	0	setting[7:0]					Vendor specific unique unit code Byte 02				
F7RC5x	0	0	1	0	1	setting[7:0]					Vendor specific unique unit code Byte 12				
F7RC6x	0	0	1	1	0	setting[7:0]					Vendor specific unique unit code Byte 22				
F7RC7x	0	0	1	1	1	setting[7:0]					Vendor specific unique unit code Byte 32				
F7RC8x	0	1	0	0	0	setting[7:0]					Vendor specific unique unit code Byte 42				
F7RC9x	0	1	0	0	1	setting[7:0]					Vendor specific unique unit code Byte 52				
F7RCAx	0	1	0	1	0	setting[7:0]					Vendor specific unique unit code Byte 62				
F7RCBx	0	1	0	1	1	setting[7:0]					Vendor ID [7:0]3				
F7RCCx	0	1	1	0	0	setting[7:0]					Vendor ID [15:8]3				
F7RCDx	0	1	1	0	1	setting[7:0]					Device ID [7:0]3				
F7RCEx	0	1	1	1	0	setting[7:0]					Device ID [15:8]3				
F7RCFx	0	1	1	1	1	setting[7:0]					Revision ID [7:0]3				

Table 29 - F0RC02: Timing and IBT Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Reserved	Reserved
x	x	x	1		Reserved
x	x	0	x	DPA Input Bus Termination Disable ¹	Enable
x	x	1	x		Disable
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

Table 30 - F0RC06: Command Space Control Word definition

Setting (DA[3:0])				Command No	Command Name	Result
0	0	0	0	CMD0	SoftReset ¹	Resets state of Media controller. Sends reset to DB for 16 * tCK. Self Clear in the next cycle. Does NOT cause QRST_n assertion.
0	0	0	1	CMD1	DB Reset	Sends reset to DB for 16 * tCK. Does NOT reset Media controller.
0	0	1	0	CMD2	Reserved	Reserved
0	0	1	1	CMD3	Reserved	Reserved
0	1	0	0	CMD4	CW Read Operation	Sends selected CW (in CW source selection control word) to MPR page 0
0	1	0	1	CMD5	CW Write Operation	Writes “data” in CW data control word to selected CW (in CW source selection control word)
0	1	1	0	CMD6	Clear Parity Error	Clear ‘CA Parity Error Status’ bit and ‘> 1 Error’ bit and re-enable parity checking (if not already enabled)
0	1	1	1	CMD7	Reserved	Reserved
1	0	0	0	CMD8	Reserved	Reserved
1	0	0	1	CMD9	Soft Media controller Reset ^{1,2,3}	Resets state of Media controller. Self Clear in the next cycle. Does NOT cause QRST_n assertion and does NOT send reset to DB.
1	0	1	0	CMD10	Reserved	Reserved
1	0	1	1	CMD11	Reserved	Reserved for future use
1	1	0	0	CMD12	Reserved	Reserved for future use
1	1	0	1	CMD13	Reserved	Reserved for future use
1	1	1	0	CMD14	Reserved	Reserved for future use
1	1	1	1	CMD15	NOP	No Operation ⁴

NOTE:

1. Requires waiting for tSTAB
2. The DDR4DB01 must not be in MPR Read override mode or BCW Read mode and the DDR4DB01 F[7:0]BC7x control word should be cleared before issuing a Soft Media controller Reset.
3. For during Soft Media controller Reset the DDR4DB01 must be in CKE Power Down Mode
4. This operation was added specifically for hosts that don't support byte writes over the I2C Bus, i.e., that have to write more than one Media-controller Control Word(MCW) at the same time.

Table 31 - F0RC09: Power Saving Settings Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Reserved	Reserved
x	x	x	1		Reserved
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
1	0	x	x	CKE Power Down Mode ¹	CKE power down with IBT ON, Q _x ODT are a function of DODTx. If RC8x DA[7:6] is configured as '00' or '01'. If RC8x DA[76] is configured as either '00' or '01', BODT is a function of DODTn.
1	1	x	x		CKE power down with IBT OFF, Q _x ODT held LOW. If the BODT output is enabled, it is held LOW.
0	x	x	x	CKE Power Down Mode Enable ²	Disabled
1	x	x	x		Enabled

NOTE:

1. The register ignores CKE Power Down mode setting when CKE Power Down is disabled by RC09 DA3.
2. The media controller shall default to CKE Power Down Mode Disabled, upon power-up.

Table 32 - F0RC0A: NVDIMM Operating Speed¹

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	$f \leq 1600 \text{ MT/s}$	DDR4-1600
x	0	0	1	$1600 \text{ MT/s} < f \leq 1866 \text{ MT/s}$	DDR4-1866
x	0	1	0	$1866 \text{ MT/s} < f \leq 2133 \text{ MT/s}$	DDR4-2133
x	0	1	1	$2133 \text{ MT/s} < f \leq 2400 \text{ MT/s}$	DDR4-2400
x	1	0	0	$2400 \text{ MT/s} < f \leq 2666 \text{ MT/s}$	DDR4-2666
x	1	0	1	$2666 \text{ MT/s} < f \leq 2933 \text{ MT/s}$	DDR4-2933
x	1	1	0	$2933 \text{ MT/s} < f \leq 3200 \text{ MT/s}$	DDR4-3200
x	1	1	1	Reserved	Reserved
0	x	x	x	Context for operation training	Default; Context 1 operation
1	x	x	x		Context 2 operation

NOTE The encoding value is used to inform the register the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a register can run.

Table 33 - F0RC0B: Operating Voltage V_{DD} and VrefCA Source Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Register V _{DD} Operating Voltage ¹	1.2V
x	x	x	1		Reserved
x	0	0	x	QVrefCA and BVrefCA Source	V _{DD} / 2 ¹ connected to QVrefCA and BVrefCA
x	0	1	x		Internally generated Vref connected to QVrefCA ² V _{DD} / 2 ¹ connected to BVrefCA
x	1	0	x		Internally generated Vref connected to BVrefCA ² V _{DD} / 2 ¹ connected to QVrefCA
x	1	1	x		External VrefCA input connected to QVrefCA and BVrefCA
0	x	x	x		Internally generated Vref ²
1	x	x	x	Input Receiver Vref Source	External VrefCA input

NOTE:

1. V_{DD} / 2 is also internally generated, but not by the VrefCA DAC.
2. Value programmed in RC1x. There is only one internal Vref generator. If more than one destination is configured for internally generated Vref, then they will all receive the same Vref level.

Table 34 - F0RC0C: Training Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	Training mode selection	Normal operating mode
x	0	0	1		Clock-to-CA training mode ¹
x	0	1	0		DCS0_n loopback mode ¹
x	0	1	1		Reserved
x	1	0	0		DCKE0_n loopback mode ¹
x	1	0	1		Reserved
x	1	1	0		DODT0_n loopback mode ¹
x	1	1	1		Reserved
0	x	x	x	Reserved for future use	Reserved for future use
1	x	x	x		Reserved for future use

NOTE In these training modes the Media controller 01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals).

Table 35 - F0RC0D: DIMM Configuration Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	Reserved	Reserved
x	x	0	1		Reserved
x	x	1	0		Reserved
x	x	1	1		Reserved
x	0	x	x	DIMM Type	LRDIMM
x	1	x	x		Reserved
0	x	x	x	Address mirroring for MRS commands	Disabled
1	x	x	x		Reserved

Table 36 - F0RC0E: Parity and ALERT Configuration Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Parity Enable	Parity checking disabled ¹
x	x	x	1		Parity checking enabled. Command ² must be delayed ^{3,4}
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
x	0	x	x	ALERT_n Assertion ⁵	ALERT_n stays asserted until 'Clear CA Parity Error' command is sent
x	1	x	x		ALERT_n pulse width according to Table 9
0	x	x	x	ALERT_n Re-enable ⁶	Parity checking remains disabled after ALERT_n pulse
1	x	x	x		Parity checking is re-enabled after ALERT_n pulse

NOTE:

1. Register does not check for parity including control word programming.
2. Command includes A0 .. A17, BA0 .. BA1, BG0 .. BG1, ACT_n, C0 .. C2, CKE0, ODT0, CS0_n .. CS3. It also includes BCOM[3:0], BODT and BCKE if the buffer control bus is enabled.
3. As specified in Table 128
4. At least 1 nCK for $\leq 2400\text{MT/s}$; at least 2 nCK for $> 2400\text{MT/s}$
5. This bit only affects ALERT_n assertion that is a result of a CA parity error. In case of a LOW level on the ERROR_IN_n input, ALERT_n stays asserted as long as ERROR_IN_n remains LOW unless DRST_n is LOW or the device is in clock stopped power down mode.
6. CA Parity Error Status bit in Error Log Register remains set until cleared by sending a Clear CA Parity Error command.

Table 37 - F0RC0F: Command Latency Adder Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	Latency adder nLadd to all NVDIMM-P commands	1 nCK latency adder to command
x	0	0	1		2 nCK latency adder to command
x	0	1	0		3 nCK latency adder to command
x	0	1	1		4 nCK latency adder to command
x	1	0	0		0 nCK latency adder ^{3,4}
x	1	0	1		Reserved for future use
x	1	1	0		Reserved for future use
x	1	1	1		Reserved for future use
0	x	x	x	Reserved for future use	Reserved for future use
1	x	x	X		Reserved for future use

NOTE:

1. The correct frequency range has to be programmed in RC0A before any changes to RC0F from the power-on default are allowed
2. Only valid if parity checking is disabled

Table 38 - F0RC1x: Internal VrefCA Control Word

Cmd (DA[7:0])								VrefCA as % of VDD1	Comment
0	0	0	0	0	0	0	0	50.0%	$V_{DD}/2$
0	0	0	0	0	0	0	1	50.83%	$V_{DD}/2 + 0.833\%$
0	0	0	0	0	0	1	0	51.67%	$V_{DD}/2 + 1.67\%$
0	0	0	0	0	0	1	1	52.60%	$V_{DD}/2 + 2.60\%$
0	0	0	0	0	1	0	0	53.33%	$V_{DD}/2 + 3.33\%$
0	0	0	0	0	1	0	1	54.17%	$V_{DD}/2 + 4.17\%$
0	0	0	0	0	1	1	0	55.00%	$V_{DD}/2 + 5.00\%$
0	0	0	0	0	1	1	1	55.83%	$V_{DD}/2 + 5.83\%$
0	0	0	0	1	0	0	0	56.67%	$V_{DD}/2 + 6.67\%$
0	0	0	0	1	0	0	1	57.50%	$V_{DD}/2 + 7.50\%$
0	0	0	0	1	0	1	0	58.33%	$V_{DD}/2 + 8.33\%$
0	0	0	0	1	0	1	1	59.17%	$V_{DD}/2 + 9.17\%$
0	0	0	0	1	1	0	0	60.00%	$V_{DD}/2 + 10.00\%$
0	0	0	0	1	1	0	1	60.83%	$V_{DD}/2 + 10.83\%$
0	0	0	0	1	1	1	0	61.67%	$V_{DD}/2 + 11.67\%$
0	0	0	0	1	1	1	1	62.50%	$V_{DD}/2 + 12.503\%$
0	0	0	1	0	0	0	0	63.33%	$V_{DD}/2 + 13.33\%$
0	0	0	1	0	0	0	1	64.17%	$V_{DD}/2 + 14.17\%$
0	0	0	1	0	0	1	0	65.00%	$V_{DD}/2 + 15.00\%$
0	0	0	1	0	0	1	1	65.83%	$V_{DD}/2 + 15.83\%$

0	0	0	1	0	1	0	0	66.67%	$V_{DD}/2 + 16.67\%$
0	0	0	1	0	1	0	1	Reserved	Reserved for future use
0	0	0	1	0	1	1	0	Reserved	Reserved for future use
0	0	0	1	0	1	1	1	Reserved	Reserved for future use
0	0	0	1	1	x	x	x	Reserved	Reserved for future use
0	0	1	0	0	x	x	x	Reserved	Reserved for future use
0	0	1	0	1	0	x	x	Reserved	Reserved for future use
0	0	1	0	1	1	0	0	33.33%	$V_{DD}/2 - 16.67\%$
0	0	1	0	1	1	0	1	34.17%	$V_{DD}/2 - 15.83\%$
0	0	1	0	1	1	1	0	35.00%	$V_{DD}/2 - 15.00\%$
0	0	1	0	1	1	1	1	35.83%	$V_{DD}/2 - 14.17\%$
0	0	1	1	0	0	0	0	36.67%	$V_{DD}/2 - 13.33\%$
0	0	1	1	0	0	0	1	37.50%	$V_{DD}/2 - 12.50\%$
0	0	1	1	0	0	1	0	38.33%	$V_{DD}/2 - 11.67\%$
0	0	1	1	0	0	1	1	39.17%	$V_{DD}/2 - 10.833\%$
0	0	1	1	0	1	0	0	40.00%	$V_{DD}/2 - 10.00\%$
0	0	1	1	0	1	0	1	40.83%	$V_{DD}/2 - 9.17\%$
0	0	1	1	0	1	1	0	41.67%	$V_{DD}/2 - 8.33\%$
0	0	1	1	0	1	1	1	42.50%	$V_{DD}/2 - 7.50\%$
0	0	1	1	1	0	0	0	43.33%	$V_{DD}/2 - 6.67\%$
0	0	1	1	1	0	0	1	44.17%	$V_{DD}/2 - 5.83\%$
0	0	1	1	1	0	1	0	45.00%	$V_{DD}/2 - 5.00\%$
0	0	1	1	1	0	1	1	45.83%	$V_{DD}/2 - 4.17\%$
0	0	1	1	1	1	0	0	46.67%	$V_{DD}/2 - 3.33\%$
0	0	1	1	1	1	0	1	47.50%	$V_{DD}/2 - 2.50\%$
0	0	1	1	1	1	1	0	48.33%	$V_{DD}/2 - 1.67\%$
0	0	1	1	1	1	1	1	49.17%	$V_{DD}/2 - 0.833\%$
0	1	x	x	x	x	x	x	Reserved	Reserved for future use
1	0	x	x	x	x	x	x	Reserved	Reserved for future use
1	1	x	x	x	x	x	x	Reserved	Reserved for future use

NOTE These are targetVrefCA values. Acceptable actual values are determined based on tolerances defined in electrical section.

Table 39 - F0RC2x: I²C Bus Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	I ² C Bus Interface Disabled	I ² C Bus interface is enabled
x	x	x	x	x	x	x	1		I ² C Bus interface is disabled. Media controller will not claim or acknowledge any access to its I ² C Bus address space.
x	x	x	x	x	x	0	x	I ² C Bus Read Access Control to function space 0	I ² C Bus read accesses from FN0 return data
x	x	x	x	x	x	1	x		I ² C Bus reads from FN0 return all ones ¹
x	x	x	x	x	0	x	x	I ² C Bus Write Access Control to function space 0	I ² C Bus write accesses to FN0 are executed
x	x	x	x	x	1	x	x		I ² C Bus writes to FN0 are not acknowledged and not executed
x	x	x	x	0	x	x	x	I ² C Bus Read Access Control to function spaces 1 to 7	I ² C Bus read accesses from FN1-7 return data
x	x	x	x	1	x	x	x		I ² C Bus reads from FN1-7 return all ones ¹
x	x	x	0	x	x	x	x	I ² C Bus Write Access Control to function spaces 1 to 7	I ² C Bus write accesses to FN1-7 are executed
x	x	x	1	x	x	x	x		I ² C Bus writes to FN1-7 are not acknowledged and not executed
x	x	0	x	x	x	x	x	F0RC4x CW Source Selection Context for Media controller	Context 1 (Function space 0 -7)
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE Media controller returns the status of “Internal Target Abort”. The host controller should not try to access this through I²C Bus. However, if the host ignores this then Media controller will return all ones.

Table 40 - F0RC3x: Fine Granularity NVDIMM Operating Speed¹

Setting (DA[7:0])								Definition	Encoding ²
x	0	0	0	0	0	0	0	Fine Granularity Operating Speed ^{3,4,5}	1240 MT/s < f ≤ 1260 MT/s
x	0	0	0	0	0	0	1		1260 MT/s < f ≤ 1280 MT/s
x	0	0	0	0	0	1	0		1280 MT/s < f ≤ 1300 MT/s
x	0	0	0	0	0	1	1		1300 MT/s < f ≤ 1320 MT/s
x	0	0	0	0	1	0	0		1320 MT/s < f ≤ 1340 MT/s
x	0	0	0	0	1	0	1		1340 MT/s < f ≤ 1360 MT/s
x	0	0	0	0	1	1	0		1360 MT/s < f ≤ 1380 MT/s
x	0	0	0	0	1	1	1		1380 MT/s < f ≤ 1400 MT/s
x	0	0	0	1	0	0	0		1400 MT/s < f ≤ 1420 MT/s
x	0	0	0	1	0	0	1		1420 MT/s < f ≤ 1440 MT/s
x	0	0	0	1	0	1	0		1440 MT/s < f ≤ 1460 MT/s
x	0	0	0	1	0	1	1		1460 MT/s < f ≤ 1480 MT/s
x	0	0	0	1	1	0	0		1480 MT/s < f ≤ 1500 MT/s
x	0	0	0	1	1	0	1		1500 MT/s < f ≤ 1520 MT/s
x	0	0	0	1	1	1	0		1520 MT/s < f ≤ 1540 MT/s
x	0	0	0	1	1	1	1		1540 MT/s < f ≤ 1560 MT/s
x	0	0	1	0	0	0	0		1560 MT/s < f ≤ 1580 MT/s
x	0	0	1	0	0	0	1		1580 MT/s < f ≤ 1600 MT/s
x	0	0	1	0	0	1	0		1600 MT/s < f ≤ 1620 MT/s
x	0	0	1	0	0	1	1		1620 MT/s < f ≤ 1640 MT/s
x	0	0	1	0	1	0	0		1640 MT/s < f ≤ 1660 MT/s
x	0	0	1	0	1	0	1		1660 MT/s < f ≤ 1680 MT/s
x	0	0	1	0	1	1	0		1680 MT/s < f ≤ 1700 MT/s
x	0	0	1	0	1	1	1		1700 MT/s < f ≤ 1720 MT/s
x	0	0	1	1	0	0	0		1720 MT/s < f ≤ 1740 MT/s
x	0	0	1	1	0	0	1		1740 MT/s < f ≤ 1760 MT/s
x	0	0	1	1	0	1	0		1760 MT/s < f ≤ 1780 MT/s

x	0	0	1	1	0	1	1		1780 MT/s < f ≤ 1800 MT/s
x	0	0	1	1	1	0	0		1800 MT/s < f ≤ 1820 MT/s
x	0	0	1	1	1	0	1		1820 MT/s < f ≤ 1840 MT/s
x	0	0	1	1	1	1	0		1840 MT/s < f ≤ 1860 MT/s
x	0	0	1	1	1	1	1		1860 MT/s < f ≤ 1880 MT/s
x	0	1	0	0	0	0	0		1880 MT/s < f ≤ 1900 MT/s
x	0	1	0	0	0	0	1		1900 MT/s < f ≤ 1920 MT/s
x	0	1	0	0	0	1	0		1920 MT/s < f ≤ 1940 MT/s
x	0	1	0	0	0	1	1		1940 MT/s < f ≤ 1960 MT/s
x	0	1	0	0	1	0	0		1960 MT/s < f ≤ 1980 MT/s
x	0	1	0	0	1	0	1		1980 MT/s < f ≤ 2000 MT/s
x	0	1	0	0	1	1	0		2000 MT/s < f ≤ 2020 MT/s
x	0	1	0	0	1	1	1		2020 MT/s < f ≤ 2040 MT/s
x	0	1	0	1	0	0	0		2040 MT/s < f ≤ 2060 MT/s
x	0	1	0	1	0	0	1		2060 MT/s < f ≤ 2080 MT/s
x	0	1	0	1	0	1	0		2080 MT/s < f ≤ 2100 MT/s
x	0	1	0	1	0	1	1		2100 MT/s < f ≤ 2120 MT/s
x	0	1	0	1	1	0	0		2120 MT/s < f ≤ 2140 MT/s
x	0	1	0	1	1	0	1		2140 MT/s < f ≤ 2160 MT/s
x	0	1	0	1	1	1	0		2160 MT/s < f ≤ 2180 MT/s
x	0	1	0	1	1	1	1		2180 MT/s < f ≤ 2200 MT/s
x	0	1	1	0	0	0	0		2200 MT/s < f ≤ 2220 MT/s
x	0	1	1	0	0	0	1		2220 MT/s < f ≤ 2240 MT/s
x	0	1	1	0	0	1	0		2240 MT/s < f ≤ 2260 MT/s
x	0	1	1	0	0	1	1		2260 MT/s < f ≤ 2280 MT/s
x	0	1	1	0	1	0	0		2280 MT/s < f ≤ 2300 MT/s
x	0	1	1	0	1	0	1		2300 MT/s < f ≤ 2320 MT/s
x	0	1	1	0	1	1	0		2320 MT/s < f ≤ 2340 MT/s

x	0	1	1	0	1	1	1	2340 MT/s < f ≤ 2360 MT/s
x	0	1	1	1	0	0	0	2360 MT/s < f ≤ 2380 MT/s
x	0	1	1	1	0	0	1	2380 MT/s < f ≤ 2400 MT/s
x	0	1	1	1	0	1	0	2400 MT/s < f ≤ 2420 MT/s
x	0	1	1	1	0	1	1	2420 MT/s < f ≤ 2440 MT/s
x	0	1	1	1	1	0	0	2440 MT/s < f ≤ 2460 MT/s
x	0	1	1	1	1	0	1	2460 MT/s < f ≤ 2480 MT/s
x	0	1	1	1	1	1	0	2480 MT/s < f ≤ 2500 MT/s
x	0	1	1	1	1	1	1	2500 MT/s < f ≤ 2520 MT/s
x	1	0	0	0	0	0	0	2520 MT/s < f ≤ 2540 MT/s
x	1	0	0	0	0	0	1	2540 MT/s < f ≤ 2560 MT/s
x	1	0	0	0	0	1	0	2560 MT/s < f ≤ 2580 MT/s
x	1	0	0	0	0	1	1	2580 MT/s < f ≤ 2600 MT/s
x	1	0	0	0	1	0	0	2600 MT/s < f ≤ 2620 MT/s
x	1	0	0	0	1	0	1	2620 MT/s < f ≤ 2640 MT/s
x	1	0	0	0	1	1	0	2640 MT/s < f ≤ 2660 MT/s
x	1	0	0	0	1	1	1	2660 MT/s < f ≤ 2680 MT/s
x	1	0	0	1	0	0	0	2680 MT/s < f ≤ 2700 MT/s
x	1	0	0	1	0	0	1	2700 MT/s < f ≤ 2720 MT/s
x	1	0	0	1	0	1	0	2720 MT/s < f ≤ 2740 MT/s
x	1	0	0	1	0	1	1	2740 MT/s < f ≤ 2760 MT/s
x	1	0	0	1	1	0	0	2760 MT/s < f ≤ 2780 MT/s
x	1	0	0	1	1	0	1	2780 MT/s < f ≤ 2800 MT/s
x	1	0	0	1	1	1	0	2800 MT/s < f ≤ 2820 MT/s
x	1	0	0	1	1	1	1	2820 MT/s < f ≤ 2840 MT/s
x	1	0	1	0	0	0	0	2840 MT/s < f ≤ 2860 MT/s
x	1	0	1	0	0	0	1	2860 MT/s < f ≤ 2880 MT/s
x	1	0	1	0	0	1	0	2880 MT/s < f ≤ 2900 MT/s

x	1	0	1	0	0	1	1		2900 MT/s < f ≤ 2920 MT/s
x	1	0	1	0	1	0	0		2920 MT/s < f ≤ 2940 MT/s
x	1	0	1	0	1	0	1		2940 MT/s < f ≤ 2960 MT/s
x	1	0	1	0	1	1	0		2960 MT/s < f ≤ 2980 MT/s
x	1	0	1	0	1	1	1		2980 MT/s < f ≤ 3000 MT/s
x	1	0	1	1	0	0	0		3000 MT/s < f ≤ 3020 MT/s
x	1	0	1	1	0	0	1		3020 MT/s < f ≤ 3040 MT/s
x	1	0	1	1	0	1	0		3040 MT/s < f ≤ 3060 MT/s
x	1	0	1	1	0	1	1		3060 MT/s < f ≤ 3080 MT/s
x	1	0	1	1	1	0	0		3080 MT/s < f ≤ 3100 MT/s
x	1	0	1	1	1	0	1		3100 MT/s < f ≤ 3120 MT/s
x	1	0	1	1	1	1	0		3120 MT/s < f ≤ 3140 MT/s
x	1	0	1	1	1	1	1		3140 MT/s < f ≤ 3160 MT/s
x	1	1	0	0	0	0	0		3160 MT/s < f ≤ 3180 MT/s
x	1	1	0	0	0	0	1		3180 MT/s < f ≤ 3200 MT/s
x	1	1	x	x	x	1	x		Reserved for future use
x	1	1	x	x	1	x	x		Reserved for future use
x	1	1	x	1	x	x	x		Reserved for future use
x	1	1	1	x	x	x	x		Reserved for future use
0	x	x	x	x	x	x	x	Reserved for future use	Reserved for future use
1	x	x	x	x	x	x	x		Reserved for future use

NOTE:

1. This control word defines the frequency of the CK_t - CK_c input reference clock during normal operation (i.e., when not in test frequency range) in units of 20 MT/s (i.e., 10 MHz).
2. The frequency ranges shown in this column are for the base frequency of the input clock and they do not include SSC modulation effects. In some cases, due to SSC modulation, the actual frequency of the input clock can straddle two adjacent frequency ranges.
3. The encoding value is used to inform the Media controller of the operating speed that it is being run at in a system. It is not an indicator of how fast or slow an Media controller can run.
4. The Media controller is required to correctly execute Media-controller Control Word(MCW) Write commands (i.e., MRS commands) at any valid frequency before the Fine Granularity Operating Speed Control Word is programmed.
5. The host is responsible for programming RC3x with the settings corresponding to the input clock frequency before initiating any training procedures. The host is also responsible for keeping the settings in RC3x and RC0A consistent with each other.

Table 41 - F0RC4x: CW Source Selection Control Word

Setting (DA[7:0])								Definition	Encoding
0	0	0	AI 2	AI 1	AI 0	A 9	A 8	Upper CW address for CW Read or CW Write operations	CW read or write to Function space 0 (JEDEC defined)
0	0	1	AI 2	AI 1	AI 0	A 9	A 8		CW read or write to Function space 1 (vendor specific)
0	1	0	AI 2	AI 1	AI 0	A 9	A 8		CW read or write to Function space 2 (vendor specific)
0	1	1	AI 2	AI 1	AI 0	A 9	A 8		CW read or write to Function space 3 (vendor specific)
1	0	0	AI 2	AI 1	AI 0	A 9	A 8		CW read or write to Function space 4 (vendor specific)
1	0	1	AI 2	AI 1	AI 0	A 9	A 8		CW read or write to Function space 5 (vendor specific)
1	1	0	AI 2	AI 1	AI 0	A 9	A 8		CW read or write to Function space 6 (vendor specific)
1	1	1	AI 2	AI 1	AI 0	A 9	A 8		CW read or write to Function space 7 (vendor specific)

Table 42 - F0RC5x: CW Destination Selection & Write/Read Additional QxODT[1:0] Signal High

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	0	0	Reserved	Reserved
x	x	x	x	x	x	0	1		Reserved
x	x	x	x	x	x	1	0		Reserved
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	0	0	x	x	Reserved	Reserved
x	x	x	x	0	1	x	x		Reserved
x	x	x	x	1	0	x	x		Reserved
x	x	x	x	1	1	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved for future use	Reserved for future use
x	x	x	1	x	x	x	x		Reserved for future use
0	MPR bit 1	MPR bit 0	x	x	x	x	x	CW Read or Write Operation ¹	MPR address and AI bit
1	MPR bit 1	MPR bit 0	x	x	x	x	x	CW Read or Write Operation with auto- increment ^{1,2}	MPR address and AI bit

NOTE:

1. The MPR bits field (DA[6:5]) bits are only used in CMD4 CW Read Operations and are DON'T CARE for CMD5 CW Write operations
2. CW Read and CW Write commands auto-increment the address field (DA[3:0]) in the CW source selection control word by '1' and the MPR bits field (DA[6:5]) in the CW destination selection control word by '1' after the commands are executed. Auto increment is only applicable to 8b CW Reads and CW Writes.

Table 43 - F0RC6x: CW Data Control Word

Setting (DA[7:0])								Definition	Encoding ²
A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0	Content of A[7:0] for CW Write or CW Read ¹ command	CW data

NOTE The content of the A[3:0] bits for CW Read commands for 4-bit CWs is DON'T CARE and has no impact on functionality.

Table 44 - F0RC7x: IBT Control Word

Setting (DA[7:0])								Definition ¹	Encoding
x	x	x	x	x	x	0	0	CA Input Bus Termination ²	100 Ohm
x	x	x	x	x	x	0	1		150 Ohm
x	x	x	x	x	x	1	0		300 Ohm
x	x	x	x	x	x	1	1		OFF
x	x	x	x	0	0	x	x	DCS[3:0]_n Input Bus Termination ^{3,4}	100 Ohm
x	x	x	x	0	1	x	x		150 Ohm
x	x	x	x	1	0	x	x		300 Ohm
x	x	x	x	1	1	x	x		OFF
x	x	0	0	x	x	x	x	DCKE Input Bus Termination ⁵	100 Ohm
x	x	0	1	x	x	x	x		150 Ohm
x	x	1	0	x	x	x	x		300 Ohm
x	x	1	1	x	x	x	x		OFF
0	0	x	x	x	x	x	x	DODT Input Bus Termination ⁶	100 Ohm
0	1	x	x	x	x	x	x		150 Ohm
1	0	x	x	x	x	x	x		300 Ohm
1	1	x	x	x	x	x	x		OFF

NOTE:

- These are target IBT values. Acceptable actual values are determined based on tolerances defined in electrical section.
- These Media-controller Control Word(MCW) bits cover the following CA inputs: DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DC0, DC1, DC2, DPAR
- These Media-controller Control Word(MCW) bits cover the following Ctrl inputs: DCS[3:0]_n
- If the DC[1:0]/DCS[3:2]_n inputs are used for the DC[1:0] function they are not covered by RC7x, DA[3:2], but by RC7x, DA[1:0] instead
- These Media-controller Control Word(MCW) bits cover the following Ctrl inputs: DCKE0,
- These Media-controller Control Word(MCW) bits cover the following Ctrl inputs: DODT0,

Table 45 - F0RC8x: ODT Input Buffer/IBT, QxODT Output Buffer and Timing Control Word

Setting (DA[7:0])								Definition ¹	Encoding
x	x	x	x	x	x	x	0	Reserved	Reserved
x	x	x	x	x	x	x	1		Reserved
x	x	x	0	0	0	0	x	Reserved	Reserved
x	x	x	0	0	0	1	x		Reserved
x	x	x	0	0	1	0	x		Reserved
x	x	x	0	0	1	1	x		Reserved
x	x	x	0	1	0	0	x		Reserved
x	x	x	0	1	0	1	x		Reserved
x	x	x	0	1	1	0	x		Reserved
x	x	x	0	1	1	1	x		Reserved
x	x	x	1	0	0	0	x		Reserved
x	x	x	1	0	0	1	x		Reserved
x	x	x	1	0	1	0	x		Reserved
x	x	x	1	0	1	1	x		Reserved
x	x	x	1	1	0	0	x		Reserved
x	x	x	1	1	0	1	x		Reserved
x	x	x	1	1	1	0	x		Reserved
x	x	x	1	1	1	1	x		Reserved
x	x	0	x	x	x	x	x	BODT Output Driver Disabled	BODT Output Driver enabled
x	x	1	x	x	x	x	x		BODT Output Driver disabled
0	0	x	x	x	x	x	x	ODT Input buffer, Output Buffer and IBT Control	Reserved
0	1	x	x	x	x	x	x		DODT0 input buffer and IBT ON and passed to QxODT[0] output. DODT1 input buffer and IBT is OFF and QxODT1 output buffer is OFF. If F0RC8x DA5 is not set to '1', DODT0 is passed to BODT.
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

Table 46 - F0RCBx: IBT and MRS Snoop

Setting (DA[7:0])								Definition ¹	Encoding
x	x	x	x	x	x	x	0	DC0 Input Bus Termination Disable	Enabled
x	x	x	x	x	x	x	1		Disabled
x	x	x	x	x	x	0	x	DC1 Input Bus Termination Disable	Enabled
x	x	x	x	x	x	1	x		Disabled
x	x	x	x	x	0	x	x	DC2 Input Bus Termination Disable	Enabled
x	x	x	x	x	1	x	x		Disabled
x	x	x	x	0	x	x	x	DDR4DB02 MRS Snoop Disable	Enabled
x	x	x	x	1	x	x	x		Disabled
x	x	x	0	x	x	x	x	DDR4DB02 MRS Snoop Disable	Enabled
x	x	x	1	x	x	x	x		Disabled
x	x	0	x	x	x	x	x	DCKE1 Input Bus Termination Disable	Enabled
x	x	1	x	x	x	x	x		Disabled
x	0	x	x	x	x	x	x	DCKE1 Input Buffer and QxCKE1 Output Driver Disable	Enabled
x	1	x	x	x	x	x	x		Disabled
0	x	x	x	x	x	x	x	Reserved	Enabled
1	x	x	x	x	x	x	x		Disabled

5. NOTE:

1. RCD always snoops DRAM MRS command for Write/Read Preamble, Burst Length and Write CRC if F0RC8X DA[7:6] = 11.
2. If LRDIMM is enabled and F0RCBx DA3 = 0, MRS commands for DRAM MR[6:0] to Rank 0, A-side received by the DDR4RCD02 results in MRS WR command on the BCOM bus.
3. If LRDIMM is enabled and F0RCBx DA3 = 1, MRS commands for DRAM MR[6:0] to the DDR4RCD02 results in NOP command on the BCOM bus. This mode requires that the host explicitly writes to the DDR4DB02 snoop register BCWs.
4. If LRDIMM is enabled and F0RCBx DA4 = 0, the DDR4RCD02 will snoop information from MRS commands for DRAM MR[6:0] as needed for its own use.
5. If LRDIMM is enabled and F0RCBx DA4 = 1, the DDR4RCD02 will not snoop information from MRS commands for DRAM MR[6:0] for its own use. This mode requires that the host explicitly sets the snoop bits in the DDR4RCD02
6. When the input buffer is disabled, the DCKE1 input signal is assumed to be LOW by internal logic in the DDR4RCD02 If F0RC9x DA3 = 1 then the RCD will enter CKE power down state when host drives DCKE0 Low.

Table 47 - F0RCCx~ F0RCFx: CA Parity Error Log

Control Word	Setting (DA[7:0])							
F0RCCx	A7	A6	A5	A4	A3	A2	A1	A0
F0RCDx	CAS_n/ A15	WE_n /A14	A13	A12	A11	A10	A9	A8
F0RCEx	PAR	ACT_n	BG1	BG0	BA1	BA0	A17	RAS_n/ A16
F0RCFx	>1 Error ^{1,2}	CA Parity Error Status ^{1,3}	Reserved			C2	C1	C0

NOTE:

1. This bit will get reset to '0' when Clear CA Parity Error Command is sent
2. With F0RC0E DA3=1 and DA2=1, the NVDIMM-P will re-enable parity after the ALERT_n pulse. The CA Parity Error Status bit will remain set. If a subsequent parity error is detected the NVDIMM-P will re-enter the parity error state and set the '>1 Error' bit.
3. The NVDIMM-P will set this bit upon occurrence of a CA parity error.
4. For the 2 clock command such as XWRITE,XREAD with XADR, the only one command that has error is logged.

Table 48 - F1RC00: Data Buffer Interface Driver Characteristics Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	BCOM[3:0], BODT, BCKE, driver strength	Moderate Drive
x	x	x	1		Strong Drive
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
x	0	x	x	BCK_t/BCK_c driver strength	Moderate Drive
x	1	x	x		Strong Drive
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

Table 49 - F1RC05: Data Buffer Interface Output Slew Rate Control

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Slew rate control for BCOM[3:0], BODT, BCKE output drivers ¹	(Default) Moderate: Single-ended range 3 V/ns - 6 V/ns
x	x	x	1		Fast: Single-ended range 5 V/ns - 8 V/ns
x	x	0	x		Slow: Single-ended range 2 V/ns - 4 V/ns
x	x	1	x		Reserved
x	0	x	x	Slew rate control for BCK_t, BCK_c differential output drivers ¹	(Default) Moderate: Single-ended range 6 V/ns - 12 V/ns
x	1	x	x		Fast: Single-ended range 10 V/ns - 16 V/ns
0	x	x	x		Slow: Single-ended range 4 V/ns - 8 V/ns
1	x	x	x		Reserved

NOTE Slew Rate Control encodings of Moderate, Fast and Slow apply to all driver strength settings. The base range values specified in Table 68 are applicable for Ron = RZQ/17, VDD = 1.2 V and 25 °C. The Output slew rate is verified by design and characterization, and may not be subject to production test.

Table 50 - F1RC8x: BCOM[3:0]/BCKE/BODT Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Output Delay Control for BCOM[3:0], BCKE and BODT Output Signals ¹	Delay Outputs by +(0/64) * tCK (Same as Default)
x	x	x	0	0	0	0	1		Delay Outputs by +(1/64) * tCK
x	x	x	0	0	0	1	0		Delay Outputs by +(2/64) * tCK
x	x	x	...						
x	x	x	1	1	1	0	1		Delay Outputs by +(29/64) * tCK
x	x	1	1	1	1	1	0		Delay Outputs by +(30/64) * tCK
x	x	x	1	1	1	1	1		Delay Outputs by +(31/64) * tCK
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for BCOM[3:0], BCKE and BODT	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled ²

NOTE:

- These control bits do not have any effect unless F1RC8x DA7 = 1.
- When feature is enabled the delay settings in F1RC8x require a time of tODU for the delay to become stable on the outputs.

Table 51 - F1RC9x: BCK Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding	
x	x	0	0	0	0	0	0	Output Delay Control for BCK_t/BCK_c Output Signals ¹	Delay Outputs by +(0/64) * tCK (Same as Default)	
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64) * tCK	
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * tCK	
x	x	0	...							
x	x	1	1	1	1	0	1		Delay Outputs by +(29/64) * tCK	
x	x	1	1	1	1	1	0		Delay Outputs by +(30/64) * tCK	
x	x	1	1	1	1	1	1		Delay Outputs by +(31/64) * tCK	
x	0	x	x	x	x	x	x	Reserved	Reserved	
x	1	x	x	x	x	x	x		Reserved	
0	x	x	x	x	x	x	x	Output Delay Feature Enable for BCK_t/BCK_c	(Default) Feature Disabled	
1	x	x	x	x	x	x	x		Feature Enabled ²	

NOTE:

1. These control bits do not have any effect unless F1RC9x DA7 = 1.
2. When feature is enabled the delay settings in F1RC9x require a time of tODU for the delay to become stable on the outputs.

Table 52 - F2RC03: NVDIMM-P controller status

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	NVDIMM-P controller PLL/DLL locking status	Not locked.
x	x	x	1		Locked
x	x	0	x	NVDIMM-P controller initialization ready status	Not Ready
x	x	1	x		Ready
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

NOTE:

1. Host may check this status bit by I2C bus after reset and clock stopped power-down exit.
2. Host may check this status bit by I2C bus after 'internal media training start' register set @ MR6 A9.

Table 53 - F2RC3x: Power Saving Modes

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	0	0	Power Savings Mode (SREF operation)	P0 (Default)
x	x	x	x	x	x	0	1		P1
x	x	x	x	x	x	1	0		P2
x	x	x	x	x	x	1	1		P3

Table 54 - F2RC4x: Packet and timing option control

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	Metadata Burst	Disable
x	x	x	x	x	x	x	1	Ordering	Enable
x	x	x	x	x	x	0	x	tRRSE timing	0
x	x	x	x	x	x	1	x		Defined value in SPD
x	x	x	x	x	0	x	x	All-Zeros	Disable
x	x	x	x	x	1	x	x	Fail-Prevention Mode	Enable

Table 55 - F2RC5x: Correctable Channel Error Interrupt Threshold and Enable

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	Correctable Channel Error Interrupt Enable	Disable
x	x	x	x	x	x	x	1		Enable
x	x	x	x	x	x	0	x	Course/Fine Setting Select	Course value setting (4096 * Threshold multiplier)
x	x	x	x	x	x	1	x		Fine value set (64 * Threshold multiplier)
0	0	0	0	0	0	x	x	Correctable Channel Error Threshold Multiplier	0 (no threshold) ¹
...
1	1	1	1	1	1	x	x		63

NOTE When correctable channel error interrupt is enabled and threshold set to 0x00h, the NVDIMM will continue reporting correctable errors via interrupt and will wrap when reaching max counter value.

Table 56 - F2RC6x: Error Injection–Enable, Type

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	Error Timer Counter Value (units: tCK)	10b count down (1024)
x	x	x	x	x	0	0	1		12b count down (4096)
x	x	x	x	x	0	1	0		14b count down (16,384)
x	x	x	x	x	0	1	1		16b count down (65,536)
x	x	x	x	x	1	0	0		20b count down (1,048,576)
x	x	x	x	x	1	0	1		24b count down (16,777,216)
x	x	x	x	x	1	1	0		28b count down (268,435,456)
x	x	x	x	x	1	1	1		32b count down (4,294,967,296)
x	0	0	x	x	x	x	x	Error Injection Type ¹	One-shot Error Address (for Uncorrectable Media Error) ²
x	0	1	x	x	x	x	x		One-shot Error Mask ²
x	1	0	x	x	x	x	x		Timer Error Mask ³
x	1	1	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Error Injection Enable	Disabled
1	x	x	x	x	x	x	x		Enabled

NOTE:

1. Preset value for “Error Address” or “Error Mask” in F2RC7x~F2RCBx follows “Error Injection Type” setting, when the “Error Injecton Mode” is enabled.
2. One-shot Error Address/Mask injects one corresponding error.
3. Timer Error Mask injects one corresponding errors when every error timer is expires.

Table 57 - F2RC7x: Error Injection –Error Address0

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	UECC Error Address[7:0]	Address = 00h
0	0	0	0	0	0	0	1		Address = 01h
...
1	1	1	1	1	1	1	1		Address = FFh

NOTE Indicates the error type of Error Address[39:2] in F2RC7x~F2RCBx.

Table 58 - F2RC7x: Error Injection – Error Mask0

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	1	Error Mask[7:0]	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	1	x	x		CA Parity Error
x	x	x	x	1	x	x	x		Channel Read User Metadata Error
x	x	x	1	x	x	x	x		Channel Read Correctable ECC
x	x	1	x	x	x	x	x		Channel Read Uncorrectable ECC
x	1	x	x	x	x	x	x		Channel Write Correctable ECC
1	x	x	x	x	x	x	x		Channel Write Uncorrectable ECC

Table 59 - F2RC8x: Error Injection – Error Address1

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Error Address[15:8]	Address = 00h
0	0	0	0	0	0	0	1		Address = 01h
...
1	1	1	1	1	1	1	1		Address = FFh

Table 60 - F2RC8x: Error Injection – Error Mask1

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	1	Error Mask[15:8]	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	1	x	x	x	x	x		Controller Error
x	1	x	x	x	x	x	x		Write Credit Overflow
1	x	x	x	x	x	x	x		XREAD Timeout

Table 61 - F2RC9x: Error Injection – Error Address2

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Error Address[23:16]	Address = 00h
0	0	0	0	0	0	0	1		Address = 01h
...
1	1	1	1	1	1	1	1		Address = FFh

Table 62 - F2RC9x: Error Injection – Error Mask2

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	1	Error Mask[23:16]	Write Error Buffered Data
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	1	x	x	x	x		SEND Overflow
x	x	1	x	x	x	x	x		SMART Health Trip
x	1	x	x	x	x	x	x		Unconsumed Error
1	x	x	x	x	x	x	x		Thermal Warning

Table 63 - F2RCAx: Error Injection – Error Address3

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Error Address[31:24]	Address = 00h
0	0	0	0	0	0	0	1		Address = 01h
...
1	1	1	1	1	1	1	1		Address = FFh

Table 64 - F2RCAx: Error Injection – Error Mask3

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	1	Error Mask[31:24]	Vendor Specific 0
x	x	x	x	x	x	1	x		Vendor Specific 1
x	x	x	x	x	1	x	x		Vendor Specific 2
x	x	x	x	1	x	x	x		Vendor Specific 3
x	x	x	1	x	x	x	x		Vendor Specific 4
x	x	1	x	x	x	x	x		Vendor Specific 5
x	1	x	x	x	x	x	x		Vendor Specific 6
1	x	x	x	x	x	x	x		Vendor Specific 7

Table 65 - F2RCBx: Error Injection – Error Address4

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Error Address[39:32]	Address = 00h
0	0	0	0	0	0	0	1		Address = 01h
...
1	1	1	1	1	1	1	1		Address = FFh

Table 66 - F2RCBx: Error Injection – Error Mask4

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	1	Error Mask[39:32]	Vendor Specific 8
x	x	x	x	x	x	1	x		Vendor Specific 9
x	x	x	x	x	1	x	x		Vendor Specific 10
x	x	x	x	1	x	x	x		Vendor Specific 11
x	x	x	1	x	x	x	x		Vendor Specific 12
x	x	1	x	x	x	x	x		Vendor Specific 13
x	1	x	x	x	x	x	x		Vendor Specific 14
1	x	x	x	x	x	x	x		Vendor Specific 15

Table 67 - F2RCCx: Urgent Error Log – Urgent Write Error

Setting (DA[7:0])								Definition	Encoding
0	1	x	x	x	x	x	x	Write Credit Overflow	WC Overflow
1	0	x	x	x	x	x	x		PWC Overflow

Table 68 - F2RCDx: Urgent Error Log – Urgent Read Error

Setting (DA[7:0])								Definition	Encoding
0	1	x	x	x	x	x	x	RID Error	RFU
1	0	x	x	x	x	x	x		Duplicated RID

Table 69 - F2RCEx: Urgent Error Log – Error RID

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Error RID	RID = 00h
0	0	0	0	0	0	0	1		RID = 01h
...
1	1	1	1	1	1	1	1		RID = FFh (Reserved)

Table 70 - F2RCFx: Urgent Error Log – Urgent Controller Error

Setting (DA[7:0])								Definition	Encoding
0	1	x	x	x	x	x	x	Controller Error	Thermal Shutdown Error
1	0	x	x	x	x	x	x		Controller Fatal Error

Table 71 - F3RC00: Programmable READ command delay Control Word

Setting (DA[3:0])				Definition	Encoding
0	0	0	0	Programmable READ command delay	0 clk
0	0	0	1		1 clk
0	0	1	0		2 clks
0	0	1	1		3 clks
0	1	0	0		4 clks
others				Reserved	Reserved

Table 72 - F3RC01: Programmable WRITE command delay Control Word

Setting (DA[3:0])				Definition	Encoding
0	0	0	0	Programmable WRITE command delay	0 clk
0	0	0	1		1 clk
0	0	1	0		2 clks
0	0	1	1		3 clks
0	1	0	0		4 clks
others				Reserved	Reserved

Table 73 - F3RC08, F3RC09: VrefDQ Training for DQ0~3 Control Word

	Setting (DA[3:0])				Definition	Comment
F3RC08	x	x	x	1	VrefDQ Value Nibble 0	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value"
	x	x	b1	x		
	x	b2	x	x		
	b3	x	x	x		
F3RC09	x	x	x	b4	VrefDQ Range Nibble 0	Range 1 (Default) Range 2
	x	x	b5	x		
	x	0	x	x	VrefDQ Enable Nibble 0	Disabled Enabled (in training mode)
	x	1	x	x		
	0	x	x	x		
	1	x	x	x		

Table 74 - VrefDQ Training: Value

A5:A0	Range 1	Range 2	A5:A0	Range 1	Range 2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	Others	Reserved	Reserved

Table 75 - F3RC0A, F3RC0B: VrefDQ Training for DQ4~7 Control Word

	Setting (DA[3:0])				Definition	Comment
F3RC0A	x	x	x	b0	VrefDQ Value Nibble 1	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value”
	x	x	b1	x		
	x	b2	x	x		
	b3	x	x	x		
F3RC0B	x	x	x	b4	VrefDQ Range Nibble 1	Range 1 (Default)
	x	x	b5	x		
	x	0	x	x		Range 2
	x	1	x	x		
	0	x	x	x	VrefDQ Enable Nibble 1	Disabled
	1	x	x	x		Enabled (in training mode)

Table 76 - F3RC0C, F3RC0D: VrefDQ Training for DQ8~11 Control Word

	Setting (DA[3:0])				Definition	Comment
F3RC0C	x	x	x	b0	VrefDQ Value Nibble 2	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value”
	x	x	b1	x		
	x	b2	x	x		
	b3	x	x	x		
F3RC0D	x	x	x	b4	VrefDQ Range Nibble 2	Range 1 (Default)
	x	x	b5	x		
	x	0	x	x		Range 2
	x	1	x	x		
	0	x	x	x	VrefDQ Enable Nibble 2	Disabled
	1	x	x	x		Enabled (in training mode)

Table 77 - F3RC0E, F3RC0F: VrefDQ Training for DQ12~15 Control Word

	Setting (DA[3:0])				Definition	Encoding
F3RC0E	x	x	x	b0	VrefDQ Value Nibble 3	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
	x	x	b1	x		
	x	b2	x	x		
	b3	x	x	x		
F3RC0F	x	x	x	b4	VrefDQ Range Nibble 3	Range 1 (Default)
	x	x	b5	x		Range 2
	x	0	x	x		Disabled
	x	1	x	x		Enabled (in training mode)
	0	x	x	x	VrefDQ Enable Nibble 3	Disabled
	1	x	x	x		Enabled (in training mode)

Table 78 - F3RC1x: VrefDQ Training for DQ16~19 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 4	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 4	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 4	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 79 - F3RC2x: VrefDQ Training for DQ20~23 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 5	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 4	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 4	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 80 - F3RC3x: VrefDQ Training for DQ24~27 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 6	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 6	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 6	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 81 - F3RC4x: VrefDQ Training for DQ28~31 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 7	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 7	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 7	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 82 - F3RC5x: VrefDQ Training for DQ32~35 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 8	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 8	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 8	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 83 - F3RC6x: VrefDQ Training for DQ36~39 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 9	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 9	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 9	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 84 - F3RC7x: VrefDQ Training for DQ40~43 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 10	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 10	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 10	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 85 - F3RC8x: VrefDQ Training for DQ44~47 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 11	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 11	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 11	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 86 - F3RC9x: VrefDQ Training for DQ48~51 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 12	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 12	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 12	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 87 - F3RCAx: VrefDQ Training for DQ52~55 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 13	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 13	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 13	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 88 - F3RCBx: VrefDQ Training for DQ56~59 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 14	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 14	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 14	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 89 - F3RCCx: VrefDQ Training for DQ60~63 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	b0	VrefDQ Value Nibble 15	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	x	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	x	x	x		
x	x	x	b4	x	x	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 15	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 15	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 90 - F3RCDx: VrefDQ Training for CB0~3 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	X	x	b0	VrefDQ Value Nibble 16	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	X	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	X	x	x		
x	x	x	b4	x	X	x	x		
x	x	b5	x	x	X	x	x		
x	0	x	x	x	X	x	x	VrefDQ Range Nibble 16	Range 1 (Default)
x	1	x	x	x	X	x	x		Range 2
0	x	x	x	x	X	x	x	VrefDQ Enable Nibble 16	Disabled
1	x	x	x	x	X	x	x		Enabled (in training mode)

Table 91 - F3RCEx: VrefDQ Training for CB4~7 Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	X	x	b0	VrefDQ Value Nibble 17	Refer to VrefDQ training values defined in Table 74 - VrefDQ Training: Value
x	x	x	x	x	X	b1	x		
x	x	x	x	x	b2	x	x		
x	x	x	x	b3	X	x	x		
x	x	x	b4	x	X	x	x		
x	x	b5	x	x	x	x	x		
x	0	x	x	x	x	x	x	VrefDQ Range Nibble 17	Range 1 (Default)
x	1	x	x	x	x	x	x		Range 2
0	x	x	x	x	x	x	x	VrefDQ Enable Nibble 17	Disabled
1	x	x	x	x	x	x	x		Enabled (in training mode)

Table 92 - F4RC8x~F4RCEx: Event Log

Control Word	Setting (DA[7:0])				
F4RC8x	VALID	V_ADDR	RFU	RFU	TYPE[3:0]
F4RC9x	STATUS[7:0]				
F4RCAx	ADDR[7:0]				
F4RCBx	ADDR[15:8]				
F4RCCx	ADDR[23:16]				
F4RCDx	ADDR[31:24]				
F4RCEx	ADDR[39:32]				

NOTE Event Log register is automatically updated by Write ECC error, UE response of read-request and Interrupt event. The register is overwritten by mulitle Events. So it is recommended to check and clear the VALID bit after the event occurs.

Table 93 - F7RC1x: Date Code Byte 0

Setting (DA[7:0])								Definition		Encoding	
x	x	x	x	0	0	0	0	Date Code Digit 0 ^{1,2} Year Information	Digit = 0		
x	x	x	x	0	0	0	1		Digit = 1		
x	x	x	x	0	0	1	0		Digit = 2		
x	x	x	x		
x	x	x	x	0	1	1	1		Digit = 7		
x	x	x	x	1	0	0	0		Digit = 8		
x	x	x	x	1	0	0	1		Digit = 9		
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved		
x	x	x	x	...							
x	x	x	x	1	1	1	1				
0	0	0	0	x	x	x	x	Date Code Digit 1 ^{1,2} Year Information	Digit = 0		
0	0	0	1	x	x	x	x		Digit = 1		
0	0	1	0	x	x	x	x		Digit = 2		
...				x	x	x	x		...		
0	1	1	1	x	x	x	x		Digit = 7		
1	0	0	0	x	x	x	x		Digit = 8		
1	0	0	1	x	x	x	x		Digit = 9		
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved		
...				x	x	x	x				
1	1	1	1	x	x	x	x				

NOTE:

1. Programmed and locked in one time programmable memory by Media controller vendor.
2. This is year date code byte for Media controller. It must be represented in Binary Coded Decimal (BCD). For example, year 2015 would be coded as 15h (0001 0101).

Table 94 - F7RC2x: Date Code Byte 1

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Date Code Digit 2 ^{1,2} Work Week Information	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 3 ^{1,2} Work Week Information	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

NOTE:

1. Programmed and locked in one time programmable memory by Media controller vendor.
2. This is work week date code byte for Media controller. It must be represented in Binary Coded Decimal (BCD). For example, week 47 would be coded as 47h (0100 0111).

Table 95 - F7RC3x: Date Code Byte 2

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Date Code Digit 4 ¹ Reserved	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 5 ¹ Reserved	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

NOTE Programmed and locked in one time programmable memory by Media controller vendor.

Table 96 - F7RC4x: Vendor Specific Unique Unit Code Byte 0

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 0 of Unique Unit Code ¹	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE Programmed and locked in one time programmable memory by Media controller vendor.

Table 97 - F7RC5x: Vendor Specific Unique Unit Code Byte 1

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 1 of Unique Unit Code ¹	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE Programmed and locked in one time programmable memory by Media controller vendor.

Table 98 - F7RC6x: Vendor Specific Unique Unit Code Byte 2

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 2 of Unique Unit Code ¹	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE Programmed and locked in one time programmable memory by Media controller vendor.

Table 99 - F7RC7x: Vendor Specific Unique Unit Code Byte 3

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 3 of Unique Unit Code ¹	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE Programmed and locked in one time programmable memory by Media controller vendor.

Table 100 - F7RC8x: Vendor Specific Unique Unit Code Byte 4

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 4 of Unique Unit Code ¹	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE Programmed and locked in one time programmable memory by Media controller vendor.

Table 101 - F7RC9x: Vendor Specific Unique Unit Code Byte 5

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 5 of Unique Unit Code ¹	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE Programmed and locked in one time programmable memory by Media controller vendor.

Table 102 - F7RCAx: Vendor Specific Unique Unit Code Byte 6

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 6 of Unique Unit Code ¹	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE Programmed and locked in one time programmable memory by Media controller vendor.

Table 103 - F7RCBx: Vendor ID Byte 0¹

Setting (DA[7:0])	Definition	Encoding
0 0 0 0 0 0 0 0	Byte 0 of Vendor ID ²	VID[7:0] = 00h
0 0 0 0 0 0 0 1		VID[7:0] = 01h
0 0 0 0 0 0 1 0		VID[7:0] = 02h
...		...
1 1 1 1 1 0 0 1		VID[7:0] = FDh
1 1 1 1 1 1 1 0		VID[7:0] = FEh
1 1 1 1 1 1 1 1		VID[7:0] = FFh

NOTE:

1. This is a fixed vendor specific register.
2. As defined for I²C Function 0 Address 0x00.

Table 104 - F7RCCx: Vendor ID Byte 1¹

Setting (DA[7:0])	Definition	Encoding
0 0 0 0 0 0 0 0	Byte 1 of Vendor ID ²	VID[15:8] = 00h
0 0 0 0 0 0 0 1		VID[15:8] = 01h
0 0 0 0 0 0 1 0		VID[15:8] = 02h
...		...
1 1 1 1 1 0 0 1		VID[15:8] = FDh
1 1 1 1 1 1 1 0		VID[15:8] = FEh
1 1 1 1 1 1 1 1		VID[15:8] = FFh

NOTE:

3. This is a fixed vendor specific register.
4. As defined for I²C Function 0 Address 0x01.

Table 105 - F7RCDx: Device ID Byte 0¹

Setting (DA[7:0])	Definition	Encoding
0 0 0 0 0 0 0 0	Byte 0 of Device ID ²	DID[7:0] = 00h
0 0 0 0 0 0 0 1		DID[7:0] = 01h
0 0 0 0 0 0 1 0		DID[7:0] = 02h
...		...
1 1 1 1 1 0 0 1		DID[7:0] = FDh
1 1 1 1 1 1 1 0		DID[7:0] = FEh
1 1 1 1 1 1 1 1		DID[7:0] = FFh

NOTE:

1. This is a fixed vendor specific register.
2. As defined for I²C Function 0 Address 0x02.

Table 106 - F7RCEX: Device ID Byte 1¹

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 1 of Device ID ²	DID[15:8] = 00h
0	0	0	0	0	0	0	1		DID[15:8] = 01h
0	0	0	0	0	0	1	0		DID[15:8] = 02h
...									...
1	1	1	1	1	1	0	1		DID[15:8] = FDh
1	1	1	1	1	1	1	0		DID[15:8] = FEh
1	1	1	1	1	1	1	1		DID[15:8] = FFh

NOTE:

1. This is a fixed vendor specific register.
2. As defined for I²C Function 0 Address 0x03.

Table 107 - F7RCFx: Revision ID¹

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Revision ID ²	RID[7:0] = 00h
0	0	0	0	0	0	0	1		RID[7:0] = 01h
0	0	0	0	0	0	1	0		RID[7:0] = 02h
...									...
1	1	1	1	1	1	0	1		RID[7:0] = FDh
1	1	1	1	1	1	1	0		RID[7:0] = FEh
1	1	1	1	1	1	1	1		RID[7:0] = FFh

NOTE:

1. This is a fixed vendor specific register.
2. As defined for I²C Function 0 Address 04h.

3.3 Module Management Register

NVDIMM-P performs various module management operations as below.

- Catastrophic Save Operation
- Back-up Energy source management
- Non-volatile data erase
- Firmware update
- Factory default setting

However the module management features are out of this specification scope. See “Module Management Register” Specification for more details.

4. Command and Operation

4.1 Command Truth Table

This section describes the NVDIMM-P command truth table.

Table 108 - NVDIMM-P Command Truth Table

Function (Reference)	CKE_0		CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	BG1-BG0	BA1-BA0	C2-C0	A12 / BC_n	A17	A13	A11	A10 / AP	A9-A0	Notes	
	Previous	Current																
MRS	H	H	L	H	L	L	L	V	V	V	OP CODE							
XADR	H	H	L	ADDR[22:12]						X/SREAD: RID [4:0] PWRITE : WGID [4:0] XWRITE: RFU UNMAP:LENGTH[4:0]				ADDR[11:2]		2		
XWRITE	H	H	L	H	H	L	L	ADDR[39:33]		RFU		L	RFU	ADDR[32:23]		2,3		
PWRITE	H	H	L	H	H	L	L	ADDR[39:33]		WGID[7:5]		H	Persist	ADDR[32:23]		2,3		
SEND	H	H	L	H	H	L	H	RFU		RFU		L	L	RFU		3,4		
SEND-MRR	H	H	L	H	H	L	H	RFU		RFU		L	H	RFU		3		
SREAD	H	H	L	H	H	L	H	ADDR[39:33]		RID[7:5]		H	RFU	ADDR[32:23]		2,3		
XREAD	H	H	L	H	L	H	H	ADDR[39:33]		RID[7:5]		L	RFU	ADDR[32:23]		2,5		
UNMAP	H	H	L	H	L	H	H	ADDR[39:33]		L	L	L	H	OPCODE[0]	ADDR[32:23]			
FLUSH	H	H	L	H	L	H	H	RFU		H	H	L	H	Final	FL[1:0]+WGID[7:0]			
IOP1	H	H	L	H	L	H	H	RFU		L	H	H	H	RFU	RFU[2:0]+IOP TS[1:0]+IOP TU[4:0]			
MRACK-WGID	H	H	L	H	L	H	H	RFU		H	H	H	H	RFU	RFU			
NOP	H	H	L	H	H	H	H	V		V	V	V	V	V	V		10	
DESELECT	H	H	H	X	X	X	X	X		X	X	X	X	X	X			
POWER DOWN ENTRY	H	L	H	X	X	X	X	X		X	X	X	X	X	X	X IOP TS[1:0]+IOP TU[4:0]	6,11	
POWER DOWN EXIT_NCSTOP	L	H	H	X	X	X	X	X		X	X	X	X	X	X		6	
Self-Refresh Entry	H	L	L	H	L	L	H	V										7,9
Self-Refresh Exit	L	H	H	X	X	X	X	X										6,7,8,9,10
POWER DOWN EXIT_CSTOP/ Self-Refresh Exit	L	H	L	H	H	H	H	V										
ZQ Calibration Long	H	H	L	H	H	H	L	V		V	V	V	V	H	V			
ZQ Calibration Short	H	H	L	H	H	H	L	V		V	V	V	V	L	V			

NOTE:

1. V means H or L (a defined logic level), X means either “defined or undefined (like floating) logic level, RFU = Reserved for Future Use. OP=Op Code.
2. XADR or DESELECT command must immediately follow any/all XREAD, SREAD, XWRITE, or PWRITE commands.
3. On Die Termination (ODT) is controlled by ODT0
4. BA[1:0] is used for the MPR selection.
5. An XREAD with RID=FFh is a READ_STATUS command
6. POWER DOWN EXIT mode for Non-clock stopped(NCSTOP) or Clock stopped(CSTOP) shall be corresponding to the POWER DOWN ENTRY mode that is programmed by MR4 A[0] (See more detail in 8.2.1, “Non-clock Stopped Power-down” and 8.2.2, “Clock Stopped Power-down”)
7. The state of ODT does not affect the states described in Table 108. The ODT function is not available during Self-Refresh.
8. Controller guarantees Self-Refresh exit to be synchronous.
9. VPP and VREF(VrefCA) must be maintained during Self-Refresh operation.
10. The No Operation command should be used in cases when the NVDIMM-P is in Self-Refresh Exit.
11. If IOP mode 0 is disabled by MR1 A[6]=0, the IOP_TU and IOP_TS are ‘X’(floating) value.

4.1.1 Addressability

NVDIMM-P devices will support addressability up to 8TB per rank when combining the XREAD/ SREAD/ XWRITE with XADR extended address command in 2-cycle back-to-back commands

- ADDR[39:3] supports 128G addressability
- ADDR[2] specifies the 32 byte burst ordering of 64 byte read data packet.
- 64 byte access granularity (BL8 * 64 bit (8 byte) width)

4.1.2 RID

NVDIMM-P supports an 8-bit Read ID (RID[7:0]). RID is transmitted to the DIMM with SREAD, XREAD and XADR commands. The RID is returned from DIMM along with the read data on the transaction information bus. By using the RID, the NVDIMM-P supports up to 255 out-of-order read operations. RID=FFh with XREAD is reserved for the STATUS_READ operation.

4.1.3 WGID

NVDIMM-P supports an 8-bit Write Group ID (WGID[7:0]). The WGID is transmitted to the DIMM with XADR, PWRITE, and FLUSH commands. The WGID bitmap status is returned from the DIMM, on the data bus after a MRACT-WGID and SEND-MRR command sequence. WGID=FFh is reserved for valid field of WGIDs bitmap.

4.1.4 Persist

Persist bit = HIGH in the PWRITE command signifies that the last 64-byte data burst for a given WGID has been delivered. This is equivalent to following the persistent write command(s) associated to the same WGID with a FLUSH[10] command carrying the same WGID.

4.1.5 FL and Final

FLUSH field (FL[1:0] and Final) encodes the three flush modes supported by NVDIMM-P. The FLUSH command is described in 4.5, “FLUSH”.

4.1.6 IOP Time Shift (TS) and Time Unit (TU)

IOP time shift (IOP TS) and IOP time unit (IOP TU) field defines the time approved by the host for an IOP request. Detailed definition of IOP TS and IOP TU is described in 4.7.4, “IOP Time”.

4.2 CKE Truth Table

Current State ²	CKE		Command(N) ³	Action(N) ³	NOTE
	Previous Cycle(N-1) ¹	Current Cycle(N) ³			
Power Down	L	L	X	Maintain Power-Down	9,10
	L	H	DESELECT	Power Down Exit	8,9
Self-Refresh	L	L	X	Maintain Self-Refresh	10,14
	L	H	DESELECT	Self-Refresh Exit	11,12,14

NOTE:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR4 NVDIMM-P immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Command Truth Table.
8. Valid commands for Power-Down Entry and Exit are DESELECT only.
9. The Power-Down does not perform any refresh operations.
10. “X” means “don’t care” (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
11. On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
12. Valid commands for Self-Refresh Exit are DESELECT only except for Max Power Saving exit. NOP is allowed for these 2 modes.
13. Power Saving mode cannot be entered during Read or Write operations. For a detailed list of restrictions See “Power saving mode” in 8.2.
14. VPP and VREF(VrefCA) must be maintained during Self-Refresh operation.

4.3 Read Operation

The NVDIMM-P protocol supports multiple methods for requesting data from the NVDIMM-P device including both a transactional read (XREAD and SEND) and speculative read (SREAD) operation allowing for flexibility and performance optimization of the protocol.

4.3.1 XREAD and SEND

Similar to standard DRAM commands, NVDIMM-P command information encoding is provided on the rising edge of the clock. The host controller may initiate a transactional read operation by providing a Transactional Read (XREAD) command followed by an Extended Address (XADR) command. Other commands on the bus following the XREAD command other than XADR shall result in an indeterminate state

An explicit Read ID (RID≠FFh) for out-of-order transaction processing is provisioned. RID=FFh is reserved for the READ_STATUS operation and message packet ID, so it cannot be used for normal data requests.

Upon receipt of the XREAD command, the NVDIMM-P shall respond to the host by providing a 4-UI LOW pulse on the RSP_n signal when data corresponding the requested address is available in the NVDIMM-P output data buffers. The host controller may then issue the SEND command for the NVDIMM-P to request output. At a deterministic RL time later, the NVDIMM-P will output the transaction data on the data DQ bus, along with transaction status information comprised of the RID for each 64B block, write credit (WC), user-metadata and ECC encoding on the ECC DQs (See 2.2, “Data packet format”) The NVDIMM-P XREAD function for a single read operation is described in Figure 2 - NVDIMM-P XREAD Operation. The RL(Read Latency of SEND) follows JEDEC standard DDR4 LRDIMM RL timing.

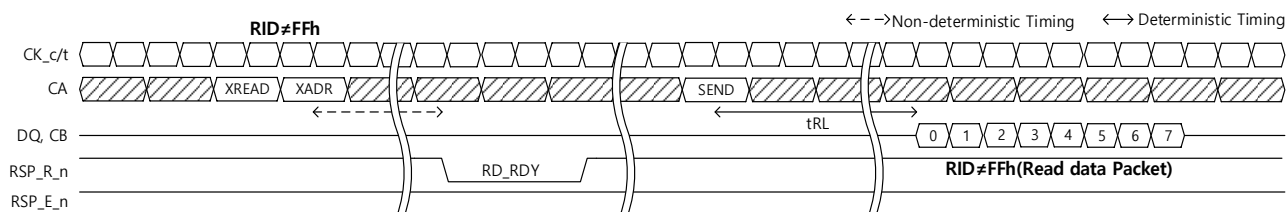


Figure 2 - NVDIMM-P XREAD Operation

NVDIMM-P transactional read operations may be issued back-to-back, enabling the commands to be “stacked” on the command/address bus. This stacking of commands reduces latency by allowing the NVDIMM-P to process the read data earlier than would be possible using the standard DRAM protocol which requires the commands to adhere to DRAM internal timing. Back-to-back XREAD operations are shown in following figure.

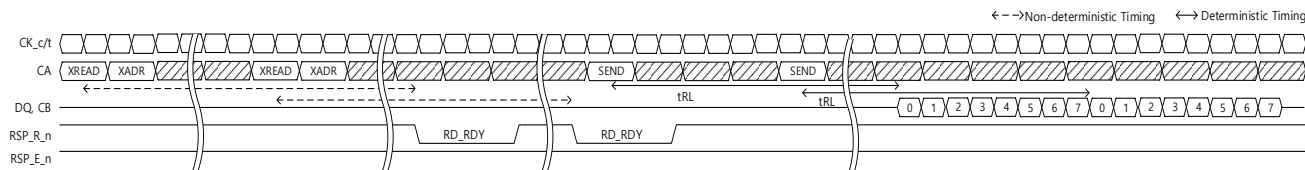


Figure 3 - Back-to-back NVDIMM-P XREAD Operations

tRRSE Timing Parameter

The DDR4 NVDIMM-P provides the tRRSE timing parameter for faster XREAD and SREAD (D_VALID=0) operation. The DDR4 NVDIMM-P knows the maximum latency for which read data will be available to transmit in a read data packet and defines the minimum tRRSE timing value to enable early notification of RD_RDY. The DDR4 NVDIMM-P minimum tRRSE timing parameter is an optional feature that can be enabled or disabled in MCW F2RC4x.

When the tRRSE timing parameter is enabled, a minimum of tRRSE is required between RD_RDY and the related SEND command to ensure valid data. The tRRSE delay is required any time RD_RDY is asserted, after XREAD/SREAD, before READ_STATUS, or with any other command operation having a RD_RDY response. An example of a XREAD operation with minimum tRRSE timing is shown in Figure 4, “- NVDIMM-P XREAD operation with minimum tRRSE timing value”.

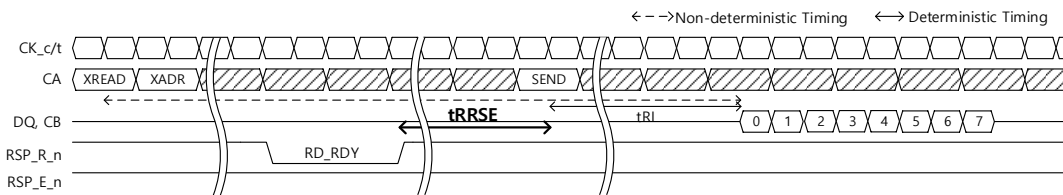


Figure 4 - NVDIMM-P XREAD operation with minimum tRRSE timing value

The minimum value of tRRSE is stored in the NVDIMM-P SPD.

4.3.2 SREAD

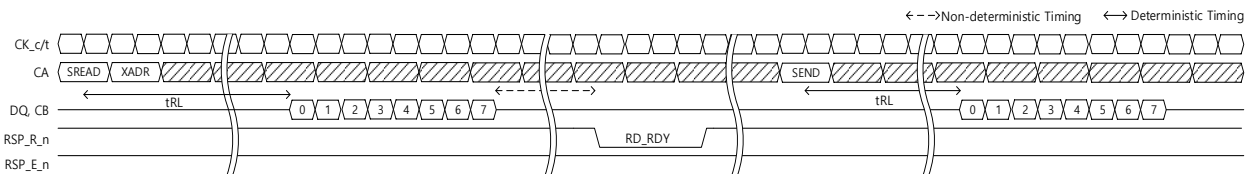
The host controller may initiate a speculative read operation by providing a Speculative Read (SREAD) command, followed by an Extended Address (XADR) command. The SREAD command must be immediately followed by the XADR command. Any other command on the bus following the SREAD command shall result in an indeterminate state.

Upon receipt of the SREAD command, immediately followed by the XADR command, the NVDIMM-P shall respond a deterministic RL time following the SREAD command with one of two responses:

1. If data corresponding to the SREAD is available in the NVDIMM-P buffers/cache, a valid read data packet shall be transferred from the NVDIMM-P with valid data on the DQ bus and D_VALID=1, WC, user-metadata, and ECC encoding on the CB bus.
2. If data corresponding to the SREAD is not available in the NVDIMM-P buffers/cache, an invalid packet (D_VALID=0) shall be transferred with invalid data on DQ bus (don't care). The NVDIMM-P shall then respond to the SREAD as if it were an XREAD by providing a RD_RDY response when the requested data is available.

And the RL(Read Latency of SREAD) follows JEDEC standard DDR4 LRDIMM RL timing.

The NVDIMM-P SREAD function is described in Figure 5.



NOTE DQS will toggle on DQ and ECC channel during a “miss” response.

Figure 5 - NVDIMM-P SREAD Operation

4.4 Write Operation

The NVDIMM-P protocol supports multiple write data functions including a transactional write (XWRITE) operation as well as a persistent write (PWRITE) operation to allow options for performance optimization and host management of persistence of data.

4.4.1 XWRITE

NVDIMM-P write operations, similar to NVDIMM-P read operations, require back-to-back commands for the write and extended addressing. The host may initiate a write operation by providing an XWRITE command, followed immediately by the XADR command. Any other command on the bus following the XWRITE-command other than XADR shall result in an indeterminate state. Following the XWRITE and XADR command combination, the host must place input data on the data bus WL time following the second beat of the XWRITE command. And the WL(Write Latency) follows JEDEC standard DDR4 LRDIMM WL timing. Once the NVDIMM-P has received the input data, and has freed the input buffer for use again, the NVDIMM-P will update write credit information, which is transferred back to the host on subsequent read or status operations. The NVDIMM-P write operation for a single XWRITE transaction is shown in Figure 6 - NVDIMM-P XWRITE Operation.

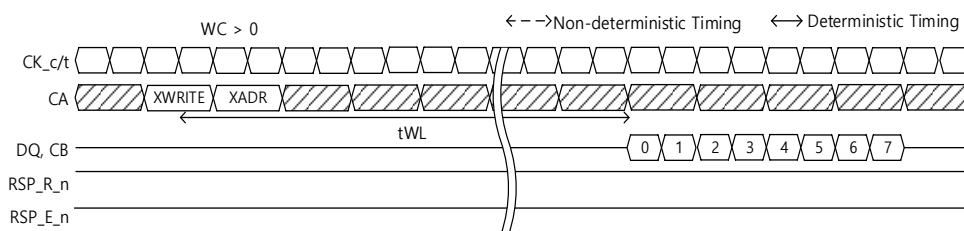


Figure 6 - NVDIMM-P XWRITE Operation

A Write Credit (WC) counter is used to limit the number of outstanding XWRITE requests that can be received the NVDIMM-P based on the available write buffer space. See more details in 6.1.2, “Write buffer management”. An example of back-to-back XWRITE commands and READ_STATUS query is shown in and Figure 7 - Back-to-back NVDIMM-P XWRITE Operation.

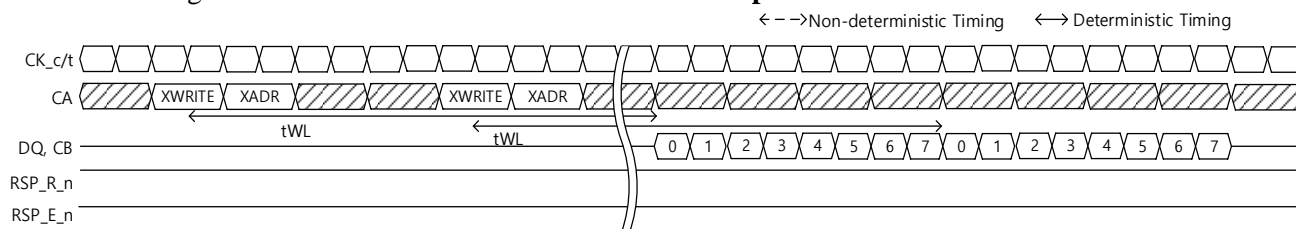


Figure 7 - Back-to-back NVDIMM-P XWRITE Operation

4.4.2 PWRITE

NVDIMM-P PWRITE commands can be used when persistence is required.

The PWRITE command is operationally similar to the XWRITE command. However, it also requires additional persistent write credits (PWC), which represents the available buffer space for PWRITE data. Therefore, a PWRITE command can be received by the NVDIMM only when both WC and PWC's are available. The NVDIMM uses the same method to return both WC and PWC's. (See more details in 6.1.2, "Write buffer management").

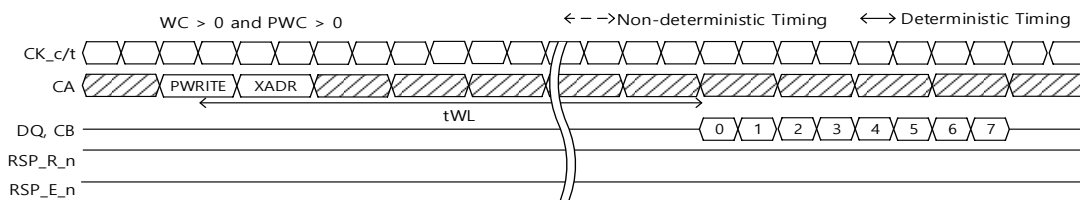


Figure 8 - NVDIMM-P PWRITE Operation

Depending on the DIMM's write group capability written in SPD, additional information can be transmitted with the PWRITE command such as Write Group ID(WGID) and a Persist bit (See more details in 6.3, "Write Data grouping"). When the additional command data is supported by the NVDIMM, the WGID tags one or more PWRITE commands and the Persist bit alerts the DIMM that the data for the specified WGID must be persisted. In this case, when the NVDIMM-P receives a PWRITE with the Persist bit set, the DIMM will respond with a W_PER response once the persist operation has completed and the data is stored in NVM. For more details see 6.3, "Write Data grouping".

4.5 FLUSH

A flush operation is provided to instruct the NVDIMM-P to move all data from cache and/or buffer space into persistent media. After tWR time from the write data transfer which need to be flushed to NVM, the FLUSH command shall be issued. Upon completion of the flush operation the NVDIMM-P will provide a flush completion response, W_PER, via RSP_E_n.

Table 109 - FLUSH command modes

FL[1]	FL[0]	WGID[7:0]	Operation
0	0	Reserved(FFh)	Flush all prior writes.
0	1	Reserved(FFh)	Flush all prior persistent writes.
1	0	Used WGID by prior PWRITE	Flush all prior persistent writes that match WGID provided with the FLUSH command.
1	1	RFU	RFU

As shown in Table 109, FLUSH field FL [1:0] indicates the three type of flush modes that are supported.

- 1) FLUSH[00] - FLUSH command with an encoding of FL[1]=0 and FL[0]=0 will cause all prior writes buffered in media controller to be pushed to NVM. All prior writes cover both PWRITEs and XWRITEs that are buffered in media controller.
- 2) FLUSH[01] - FLUSH command with an encoding of FL[1]=0 and FL[0]=1 will cause all prior PWRITEs buffered in media controller to be pushed to NVM.
- 3) FLUSH[10] - FLUSH command with an encoding of FL[1]=1 and FL[0]=0 will flush all prior PWRITEs that match the WGID provided with the FLUSH command. FLUSH[10] must be encoded with a WGID matching prior PWRITE(s) for which the persist bit has not been set yet.

When the FLUSH command is received, the NVDIMM-P moves the related write data to the NVM and sends the W_PER response once the data persistency is ensured in the NVDIMM-P. Multiple flush requests with same WGID are not allowed. Since FLUSH[00] and FLUSH[01] both use the same reserved WGID (FFh), the NVDIMM only supports one outstanding FLUSH[00] or FLUSH[01] command. Completion of a FLUSH[00] or FLUSH[01] is required before the NVDIMM can accept a new FLUSH[00] or FLUSH[01] command. .

If NVDIMM-P supports the Write Data Grouping, the NVDIMM can accept multiple FLUSH[10] commands as long as the WGID values are different. See more details in section 6.3, “Write Data grouping”.

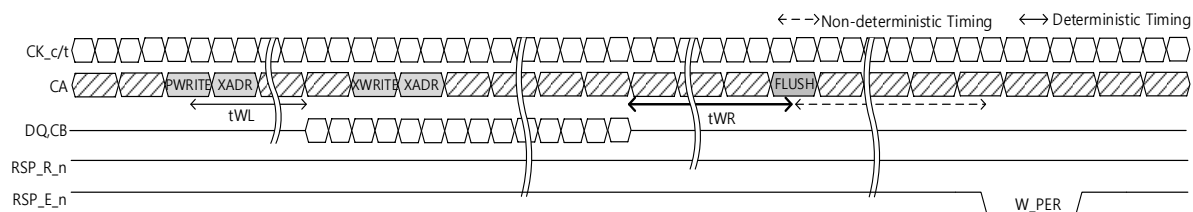


Figure 9 - The FLUSH command and completion response by W_PER.

Final Tag=1 with FLUSH command is used to push data to the NVM and saves the completion status in a non-volatile area on system power-off or a power-fail event. Regardless of previous outstanding FLUSH command, the Final FLUSH[00] or FLUSH[01] shall be issued. The flow of a Final FLUSH operation at system power loss is defined as follows:

1. All required writes have been transferred to the NVDIMM-P before the Final FLUSH command is received. Reserved WGID=FFh is used.
2. Once Final FLUSH is received and accepted without errors by the NVDIMM-P, the command/address bus must be driven to a DESELECT state. At this point the host may disable the interface.
3. The NVDIMM shall stop accepting new commands following the Final FLUSH and disable the interface
4. Power source shall be switched to back-up energy source (from System or NVDIMM-P)
5. NVDIMM-P flushes selected volatile content to NVM media
6. The completion state of Final FLUSH completion is saved in in MMR non-volatile location as Catastrophic Save Operation state. See section 3.3, “Module Management Register” for more details.\

4.6 Status register Read operation (READ_STATUS)

Upon receiving a READ_STATUS command, the NVDIMM-P will prepare the message packet, which includes NVDIMM-P status information. A READ_STATUS consists of an XREAD command immediately followed by an XADR command. A reserved RID (RID=FFh) is used to distinguish the READ_STATUS command from normal data read operation.

After receiving the READ_STATUS request, the NVDIMM-P shall respond with RD_RDY when the requested operation is completed. When a subsequent SEND command is received, the NVDIMM-P will output the message packet after a deterministic RL delay. The message packet includes the requested operation status, transferred on the DQ bus, along with the RID=FFh, POISON=0 and ECC on the CB bus. The NVDIMM-P READ_STATUS operation is described in Figure 10, “ - READ_STATUS Operation”.

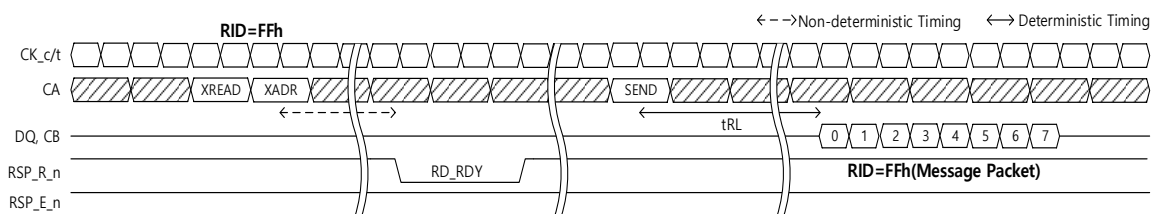


Figure 10 - READ_STATUS Operation

The encoding of the address bits, ADDR[3:2], in the XREAD/XADR command define different status information to be prepared by the NVDIMM-P and transferred in the message packet.. The other address fields are not valid in the READ_STATUS request. Detailed encodings of the ADDR[3:2] are summarized in Table 110, “ - READ_STATUS command encoding”.

Table 110 - READ_STATUS command encoding

ADDR[3:2]	Requesting Status Item in Message packet
00b	Complete the power-up initialization
01b	Available Credit synchronization (WC, PWC, CTH and UNMAP_CNT)
10b	RFU
11b	Reset RID

4.6.1 Complete the power-up initialization

After the power is up and all host trainings are completed, the NVDIMM-P controller may need more time to complete the internal initialization depending on the NVM status. The host polls the MCW F2RC03-DA[1] through the I2C bus to check the completion status or requests the NVDIMM-P to complete the initialization with READ STATUS[00](Addr[3:2]=00b). When the initialization is completed, NVDIMM-P prepares a message packet with “VALID_RDY=1 and RDY_PWR=1” and sends an RD_RDY signal to inform the host that the initialization is complete.

4.6.2 Available Credit Synchronization

During the normal operation, incremental WC and PWC for XWRTE and PWRITE are returned via the metadata bus on CB6 and CB7 pins. The NVDIMM-P also maintains the total Available WC and PWC values in the message packet, which can be used to synchronize credits on initialization or after a read or message packet ECC error which may include valid WC. Not only the available WC and PWC, but also available CTH(Credit Threshold) and UNMAP_CNT are simultaneously returned for credit synchronization. Reading the write credits values is initiated via a READ_STATUS[01](Addr[3:2]=01b). The NVDIMM-P responds with RD_RDY when the message packet is ready to be delivered. On receipt of a following SEND command, the NVDIMM will transmit the message packet (RID=FFh) including the VALID_WC=1, VALID_PWC=1, VALID_UNMAP=1 and available credit values. The Available Credit values returned in the message packet are the most recent values in the NVDIMM-P, therefore they can be used to synchronize credits across the interface.

If message packet includes Available WC and PWC, the WC and PWC in metadata bus will return '0'.

4.6.3 Reset RID

The NVDIMM-P supports a RID reset operation to discard all the pending XREADs and SREADs along with the associated RID's. Pending XREADs/SREADs are defined as commands for which data has not been transferred to the host. The Reset RID function can be used to reset the NVDIMM read data state in the case of an Uncorrectable read Channel Error or Read time-out. A Reset RID operation is initiated with a READ_STATUS[11](Addr[3:2]=11b). The command encoding is described in Table 110, " - READ_STATUS command **encoding**".

The RESET_RID operation clears not only the RID queue but also the output buffer in the NVDIMM-P. Therefore the last data packet of a SEND command response must be transferred to the host controller before a RESET RID operation is received by the NVDIMM. After a RESET_RID command is issued, any RD_RDY response shall be ignored for the duration of tRESET_RID_INIT time. During tRESET_RID_INIT, no XREAD/SREAD command is allowed.

The NVDIMM-P requires up to tRESET_RID time to reset any/all outstanding XREAD/SREADs requests in process. Upon completion of RESET_RID operation, after all prior XREADs/SREADs requests are cleared in the NVDIMM-P, a RD_RDY response is generated. After a corresponding SEND command is received, the NVDIMM-P will transfer a message packet with the VALID_RDY=1 and RID_RDY=1. Once the status bit RID_RDY=1, new XREAD/SREAD commands are allowed. The maximum RID reset time (tRESET_RID_MAX) is specified as part of SPD timing parameters.

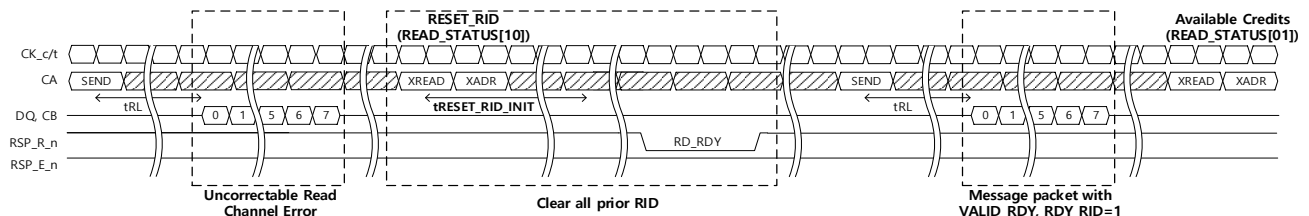


Figure 11 - NVDMM-P Reset RID operation

In the event that the host issues additional RESET_RID commands, prior RESET_RID and RD_RDY responses are ignored because of buffer and RID clear request by the last RESET_RID command, and the following rules apply:

- In the event that the host issues additional RESET_RID commands within tRESET_RID_MAX of a RESET_RID operation in progress, the NVDIMM shall respond with a single RD_RDY response as shown in Figure 12.

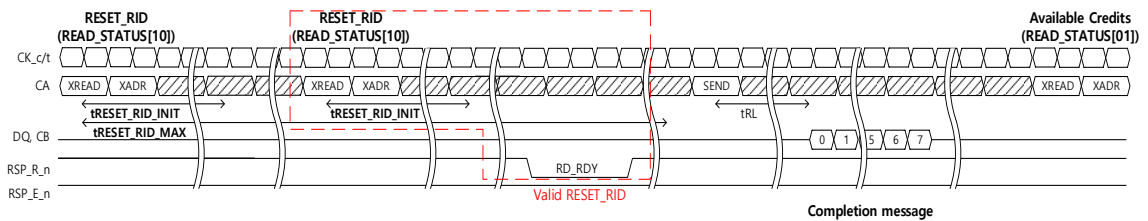


Figure 12 - Multiple Reset RID commands with single RD_RDY response case 1

- If an additional RESET_RID is initiated within tRESET_RID_MAX time of a RD_RDY response from an earlier RESET_RID, by definition, the host shall ignore the RD_RDY, and the NVDIMM shall complete a RESET_RID operation based on the second RESET_RID as in Figure 13.

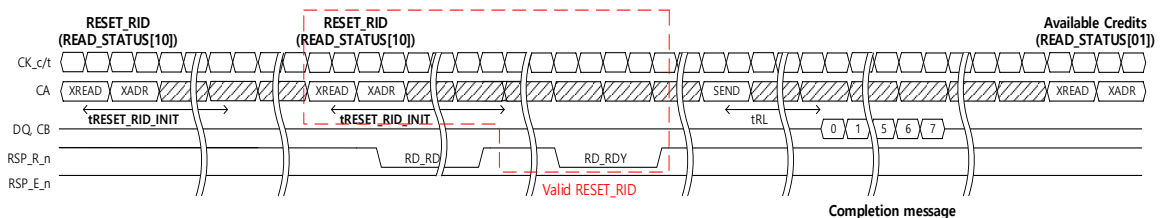


Figure 13 - Multiple Reset RID commands with additional RD_RDY response case 2

- In the case that a RESET_RID is received after a RD_RDY response, the NVDIMM-P shall return a single RD_RDY responses with RDY_RID=1 as shown in
- Figure 14. The NVDIMM-P shall continue to return RDY_RID=1 until receipt of an XWRITE command or XREAD other than a RESET_RID command completes the RESET_RID operation.

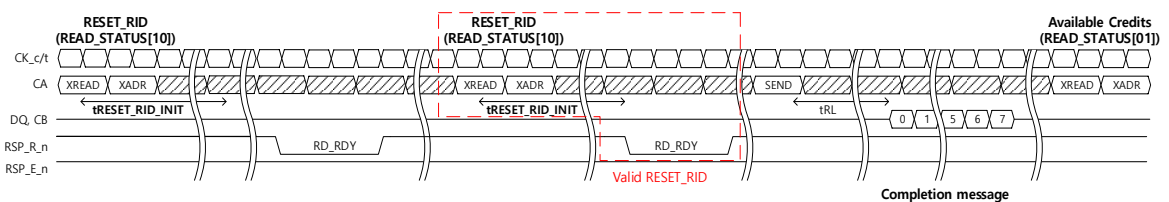


Figure 14 - Multiple Reset RID commands with additional RD_RDY response case 3

If a Read Channel Error occurs when a message packet is transferred after RESET_RID and before RD_RDY=1, the host controller may retry the RESET_RID operation.

4.7 Internal Operation (IOP)

The NVDIMM-P has an IOP request and approval mechanism to perform the NVDIMM-P Internal Operations, such as non-volatile memory media management, internal cache update, etc. When the NVDIMM-P needs the internal operation (IOP) time, the NVDIMM-P will request it to host. The host controller can approve, partially approve or reject the IOP time request. If the NVDIMM does not receive the approval command in IOP time or zero IOP time, then the IOP request is automatically rejected.

There are two IOP modes, each IOP mode can be enabled or disabled by MR1, A6 (mode 0), and A5 (mode 1) register setting separately.

4.7.1 IOP Request

The NVDIMM-P sends an IOP request to the host through following steps:

1. NVDIMM-P prepares a message packet including IOP request information in SEND command buffer queue.
2. NVDIMM-P asserts the RD_RDY signal to the host
3. Host issues SEND command to read the message packet
4. NVDIMM-P sends the message packet

Following information are included in the message packet (RID=FFh) for the IOP request:

- VALID_IOP (1 bit) : IOP request valid mark (1: valid; 0: invalid)
- Mode (1 bit) : Request IOP mode. (0:IOP 0 request, 1:IOP1 request)
- QoS (2 bits) : QoS priority (00b:Low, 01b:Medium, 10b:High, 11b:Urgent)
- IOP Time (7 bits) : IOP Time Shift (2 bits) + IOP Time Unit(5 bits)

4.7.2 IOP0 Mode

In IOP 0 Mode, the IOP0 time is approved by the host with the following steps:

1. A ‘POWER DOWN ENTRY’ command with a non-zero IOP0 time to initiate an IOP0 operation is sent to the NVDIMM-P. If the NVDIMM receives the ‘POWER DOWN ENTRY’ command with “IOP0 time”=7Fh, then it operates as a normal non-clock stopped ‘POWER DOWN ENTRY’. If the “IOP0 time” is =00h, then the IOP0 request is rejected by the host.
2. During the approved IOP0 time the command/address bus must be driven to a DESELECT state.
3. After the IOP0 time has expired, the NVDIMM will remain in a POWER DOWN state until a “POWER_DOWN_EXIT” command is received. The “POWER DOWN EXIT” command can be received immediately after IOP0 has expired.

The NVDIMM-P IOP0 operation is shown in Figure 15, “NVDIMM-P IOP Mode 0 Operation”.

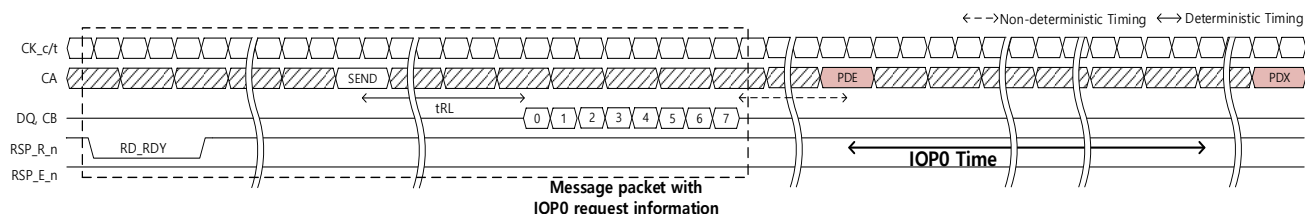


Figure 15 - NVDIMM-P IOP Mode 0 Operation

4.7.3 IOP1 Mode 1

In IOP1 Mode, the IOP1 time is approved by the host with the following steps:

1. An ‘IOP1’ command, which includes IOP1 time for approval, is sent to the NVDIMM-P.
2. During the approved IOP1 time the NVDIMM-P can still receive new commands, but the QoS of the requests during the IOP1 time may be reduced: deterministic timing should be maintained but non-deterministic response time may be elongated.
3. After IOP1 time, the behavior of the NVDIMM-P will return to normal QoS assurances.

The NVDIMM-P IOP mode-1 operation is shown in Figure 16

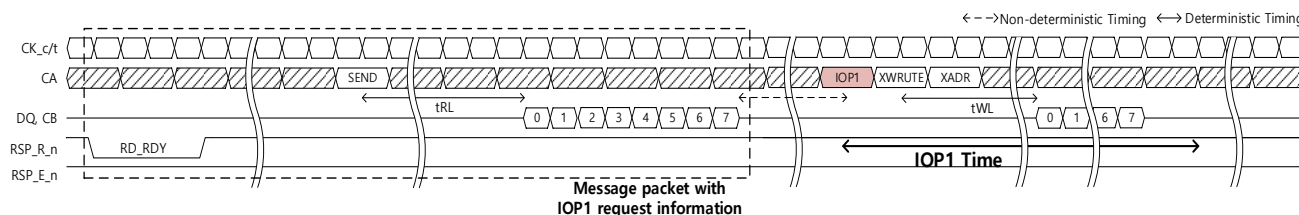


Figure 16 - NVDIMM-P IOP Mode 1 Operation

4.7.4 IOP Time

IOP time consists of two part: The first is ‘Time Shift’ and the second is ‘Time Unit’. Each time unit equals to 4 times of DDR4 DQ burst time (16tck or 32UIs). Time shift defines the number of shift value use to calculate the real IOP time. The definition of Time Shift and corresponding Shift value is described in Table 11, “IOP Shift Time Definition”.

Table 111 - IOP Shift Time Definition

Shift Time[1:0]	Shift value
00	0
01	5
10	10
11	15

By using the Shite value, the requested IOP time can be calculated as:

$$\text{Requested IOP Time} = (tCK * 16) * 2^{(\text{Shift Value})} * \text{IOP Time Unit [4:0]}$$

Then the minimum IOP intervals are summarized in Table 112, “Minimum IOP Time Intervals”.

Table 112 - Minimum IOP Time Intervals

Shift Time[1:0]	IOP time interval (clks)
00	16
01	512
10	16384
11	524288

Taking DDR4-3200 (tCK=0.625ns) for example, Table 113, “IOP Time Intervals and Ranges for DDR4-3200”, summarizes the IOP time interval and IOP time range for different Time Shift value.

Table 113 - IOP Time Intervals and Ranges for DDR4-3200

Shift Time	IOP time Interval(ns)	IOP Min Time(ns)	IOP Max Time(ns)
00	10	0	310
01	320	0	9920
10	10240	0	317440
11	327680	0	10158080

4.8 UNMAP

NVM media may require media management such as logical address, wear-leveling and garbage collection. A common way to implement these management functions is utilizing an indirection table, where the logical to physical mappings are stored.

The UNMAP command enables enhancement of media management by informing the NVDIMM-P media controller that one or several contiguous 64B blocks of data are no longer required by the host and are available for garbage collection by the media controller. Use of UNMAP can minimize latency spikes, and improve media lifetime.

The UNMAP command must be, followed immediately by an XADR command. The order and choice of execution of UNMAP commands is left to the device implementation. The host is responsible for ensuring completion of read or write operations to blocks that will be unmapped before issuing the UNMAP command.

Prior to issuing UNMAP commands, the host reads the number of UNMAP commands that NVDIMM-P controller is able to execute (Available UNMAP_CNT) by issuing READ_STATUS[01]. And the number of UNMAP commands issued by the host shall be less than or equal to the Available UNMAP_CNT.

UNMAP command includes the following information:

- ADDR[39:2]: the starting 64B block address, aligned to a 64B boundary, and
- LENGTH[4:0]: the length (zero-based, in number of 64B blocks, up to 32) of the range of memory that needs to be unmapped by the media controller. Length = LENGTH[4:0]+1.
- OPCODE[0]: defines different usages of UNMAP command, as shown in Table 114, “Definition of OPCODE for UNMAP”

Table 114 - Definition of OPCODE for UNMAP

OPCODE[0]	Meaning
0	This command only requests NVDIMM-P to unmap the corresponding data block. The content of the block are left in any state as chosen by the device implementation. After the command is completed, the original data may remain partially or fully read/write accessible to the host.
1	Reserved

5. DDR interface and Training

5.1 Command ordering

5.1.1 Read and Write Commands Ordering Rules

The following set of ordering rules apply when read and write transactions are issued to NVDIMM-P.

1. RAW (Read after Write) - Write command to address A followed by Read command to address A:

- NVDIMM-P read must return the value from the preceding Write command.
- The read(XREAD and SREAD) command to the address A shall be issued after t_{WR} time from the last write data packet to the same address A.

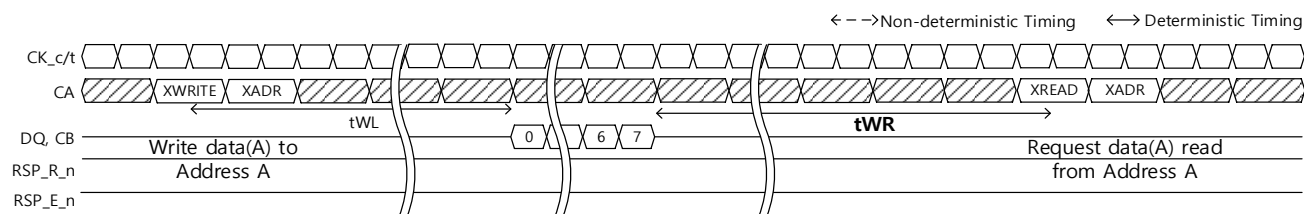


Figure 17 - RAW timing diagram

2. WAR (Write after Read) - Read command to address A followed by Write command to address A:

- The write(XWRITE and PWRITE) command to the address A shall be issued after t_{WAR} time from the last read(XREAD and SREAD) command to the same address A.
- Data ordering to same address A always follows the read(XREAD and SREAD) and write(XWRITE and PWRITE) command ordering excluding SEND command.

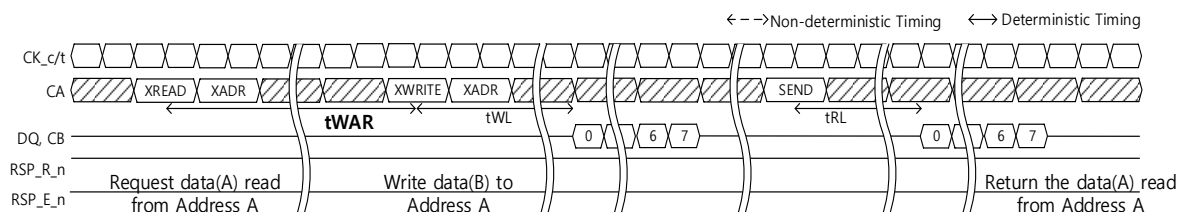


Figure 18 - WAR timing diagram

WAR (Write After Read) data ordering support:

The NVDIMM-P shall describe the capability in the SPD for supporting the preservation of data ordering in the case of a write after read data. For NVDIMMs which can honor write after read data ordering:

SUPPORTED: Following the completion of time (t_{WAR}), the NVDIMM-P shall guarantee the order for returning the data from a read operation to address A following the write of new data into address A. Subsequent read operations to address A shall return the newly written data. For a write operation occurring prior to the completion of time (t_{WAR}) the NVDIMM-P does not guarantee the data ordering.

NOT SUPPORTED: Until the read request data to the address A is returned, the write command to address A shall not be issued. If the write command is issued before the prior read data returned, the NVDIMM-P does not guarantee the later returned data ordering. The t_{WAR} parameter for this case of NVDIMM-P shall be effectively 0ns.

3. WAW (Write after Write) - A sequence of Writes to address A

- NVDIMM-P must execute and retire the Writes to the media in the same order they are received from the host. In the event of an uncorrectable error on Write, it is left to the host to figure out which writes to retry.
- If a later write to a given address is received before any preceding write to the same address is executed and retired to media, it is acceptable for the media controller to discard the preceding write.

5.1.2 Flush and Write(PWRITE and XWRITE) Commands Ordering Rules

The following ordering rules apply when FLUSHs and Writes (PWRITE or XWRITE) commands are issued to NVDIMM-P:

1. Write(XWRITE or PWRITE) to FLUSH commands.

- A sequence of Write (PWRITE and/or XWRITE) commands to different addresses may be executed and retired by NVDIMM-P in any order
- The FLUSH command shall be issued after tWR time from the prior write data packet that is flushed.

2. FLUSH to FLUSH command.

- Multiple outstanding FLUSH[10] with distinct WGIDs are allowed to execute these concurrently to the media. In the case of FLUSH[00] and FLUSH[01] using reserved(FFh) WGID, only one FLUSH[00] or FLUSH[01] is allowed at a time.
- The last FLUSH[00] (FLUSH all) command completion implies that prior FLUSH[00] (FLUSH all), FLUSH[01] (FLUSH all PWRITEs) and FLUSH[10] (FLUSH PWRITEs with matched WGID) commands have also been flushed to the media.
- The last FLUSH[01] (FLUSH all PWRITEs) completion implies that prior FLUSH[01] (FLUSH all PWRITEs) and FLUSH[10] (FLUSH PWRITEs with matched WGID) commands have also been flushed to the media.

3. FLUSH to Write(XWRITE or PWRITE) command

- Any PWRITE command that is not associated with an outstanding FLUSH is allowed as long as Write Credits and PWRITE Credits are available. Once FLUSH with WGID A is issued, any PWRITE command with WGID A shall not be issued until the WGID is released by FLUSH completion.

5.2 Data and Metadata burst ordering

5.2.1 Data Burst Ordering Rule

Data burst re-ordering support is advertised in the NVDIMM SPD. When supported, address bit ADDR[2] specifies the burst start address for XREAD and SREAD commands.

- If ADDR[2]=0 then BL8 data is delivered without any reordering.
- If ADDR[2]=1 then 2nd half of BL8 data is delivered in first 4UI's and 1st half of data is delivered in last 4UI's.
- If support for data-burst re-ordering is not provided, then ADDR[2] becomes a “don't care”, and data is delivered without re-ordering

Value of ADDR[2] bit does not impact the ordering of metadata fields.

ECC bits are computed after data is reordered. ECC bits for each 4UI should represent the data and metadata transmitted in the same 4UI.

Table 115 - Burst Order by XREAD ADDR[2]

ADDR[2]		UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
0	DQ0~DQ63	0	1	2	3	4	5	6	7
	CB0~CB5	ECC				ECC			
	CB6 ¹	USER	USER	USER	USER	RID[3]	RID[2]	RID[1]	RID[0]
	CB7 ¹	POISON	WC[2]	WC[1]	WC[0]	RID[7]	RID[6]	RID[5]	RID[4]
1	DQ0~DQ63	4	5	6	7	0	1	2	3
	CB0~CB5	ECC				ECC			
	CB6 ¹	USER	USER	USER	USER	RID[3]	RID[2]	RID[1]	RID[0]
	CB7 ¹	POISON	WC[2]	WC[1]	WC[0]	RID[7]	RID[6]	RID[5]	RID[4]

NOTE Order of metadata transferred on CB6-7 is determined by MCW F2RC4x DA[0]. Table illustrates order when DA[0]=0.

For write commands, the BL8 data is always delivered without any reordering, regardless of the ADDR[2] value.

5.2.2 Metadata Burst Ordering Rule

MCW F2RC4x DA[0] shall be set to determine the burst ordering for metadata lanes CB6 and CB7 during boot time.

- If bit DA[0]=0 then metadata bits in lanes CB6 and CB7 are delivered with poison, user defined and write credits in the first half of the transfer and RID bits in the second half of the transfer.
- If bit DA[0]=1 then metadata bits in lane CB6 and CB7 are delivered with RID bits in the first half of the transfer and poison, user defined and write credits in the second half of the transfer.

For write commands, the user-defined metadata follows the same rule as read packet.

Table 116 – Option-A format example by MCW F2RC4x DA[0] setting

MCW F2RC4x DA[0]		UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
0	DQ0~DQ63	User Data				User Data			
	CB0~CB5	ECC				ECC			
	CB6 ¹	USER	USER	USER	USER	RID[3]	RID[2]	RID[1]	RID[0]
	CB7 ¹	POISON	WC[2]	WC[1]	WC[0]	RID[7]	RID[6]	RID[5]	RID[4]
1	DQ0~DQ63	User Data				User Data			
	CB0~CB5	ECC				ECC			
	CB6 ¹	RID[3]	RID[2]	RID[1]	RID[0]	USER	USER	USER	USER
	CB7 ¹	RID[7]	RID[6]	RID[5]	RID[4]	POISON	WC[2]	WC[1]	WC[0]

Refer to 2.2 for detailed metadata definition.

5.3 DLL on/off mode and switching procedure

The NVDIMM-P supports DLL on/off procedure.

Refer to the “*JESD79-4B, DDR4 SDRAM Specification, 4.4 DLL-off Mode and DLL on/off Switching procedure*” and “*JESD79-4B, DDR4 SDRAM Specification, 4.5 DLL-off Mode*” for more information.

5.4 Input Clock Frequency Change

The NVDIMM-P supports input clock frequency change.

Refer to JESD79-4B for more information.

5.5 Dual Frequency Mode

The NVDIMM-P supports dual frequency mode.

Refer to the “*JESD82-31, DDR4 Registering Clock Driver – DDR4RCD01 Specification*”

5.6 Write Leveling

Refer to the “*JESD79-4B, DDR4 SDRAM Specification, 4.7 Write Leveling*”.

Refer to the “*DDR4 DB Specification, 2.1.8 Training Support Features*”.

5.7 Multi-Purpose Register

Refer to the “*JESD79-4B, DDR4 SDRAM Specification, 4.10 Multi Purpose register*”.

5.8 ZQ Calibration Commands

Refer to the “*JESD79-4B, DDR4 SDRAM Specification, 4.12 ZQ Calibration Commands*”.

Refer to the “*DDR4 DB, Specification, 2.1.8 Training Support Features*”

5.9 DQ Vref Training

Refer to the “*JESD79-4B, DDR4 SDRAM Specification*”.

However, each 8-bits of VrefDQ Training registers are defined at F3RC08~F3RCEx. Especially the F3RC08~ F3RC0F, 4 bits register, shall always be updated 8-bits together. Therefore once MCW command for 4 bit LSB is issued, and then the next MCW command for 4bit MSB shall be immediately followed after tMRD time.

Refer to the “*JESD79-4B, DDR4 SDRAM Specification, 4.13 DQ Vref Training*”.

Refer to the “*DDR4 DB Specification, 2.1.8 Training Support Features*”.

5.10 Command Address Parity (CA Parity)

The NVDIMM-P device shall employ the same scheme for command/address bus parity as defined by the DDR4 RCD specification.

Refer to the “*JESD82-31, DDR4 Registering Clock Driver – DDR4RCD01 Specification, 2.4 Parity*”

Specific to NVDIMM-P, when a CA Parity error is detected on an XADR command, the previous associated command (XWRITE, PWRITE, XREAD, SREAD, UNMAP) will not be executed. The Qx outputs referenced in the RCD specification refer to the outputs of the on-DIMM CA parity check on the NVDIMM-P, which could be outputs of an explicit RCD device or outputs of logic within an on-DIMM media controller.

5.11 Programmable Preamble & Postamble

Refer to the “*JESD79-4B, DDR4 SDRAM Specification, 4.20 Programmable Preamble*”.

Refer to the “*JESD79-4B, DDR4 SDRAM Specification, 4.21 Postamble*”.

5.12 Programmable Command Delay

The NVDIMM-P media controller has programmable registers to provide additional command delay in order to match LRDIMM latency behavior from the HOST perspective. There are two independent delay controls, one for WRITES and one for READS. These programmable delays are applied after Latency Adder (nLadd) as shown in following figure.

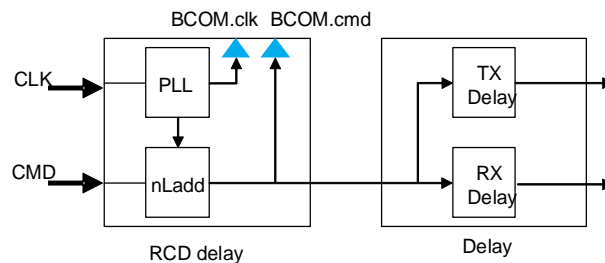


Figure 19 - Delay elements for reads and writes

There is only one register required for WRITE and one for READ to program command delay. These are used to compensate the farthest data buffer routing mismatch in addition to the RCD propagation and latency adder delays. BCOM generation is not affected by these additional command delays. The mismatches between this farthest data buffer and the remaining data buffers are adjusted using existing buffer control words F0BCDx (for write) and F0BCCx (for read). With the data buffer requirement in DB02, the routing requirement between these data buffers to NVDIMM-P controller is demonstrated in following figure. Given that both F0BCDx and F0BCCx allow up to 2tck clock adjustment, the maximum routing delay difference between the NVDIMM-P controller to the farthest data buffer (DB-A) and the NVDIMM-P controller to the closest data buffer (DB-E) should be less than 1250ps

Given clock period of 3200MT/s is 625ps. 2tck clock adjustment is 1250ps

$$(tBCK_A + tBCK_B + tBCK_C + tBCK_D + tMDQS_A) - (tMDQS_E) \leq 1250ps$$

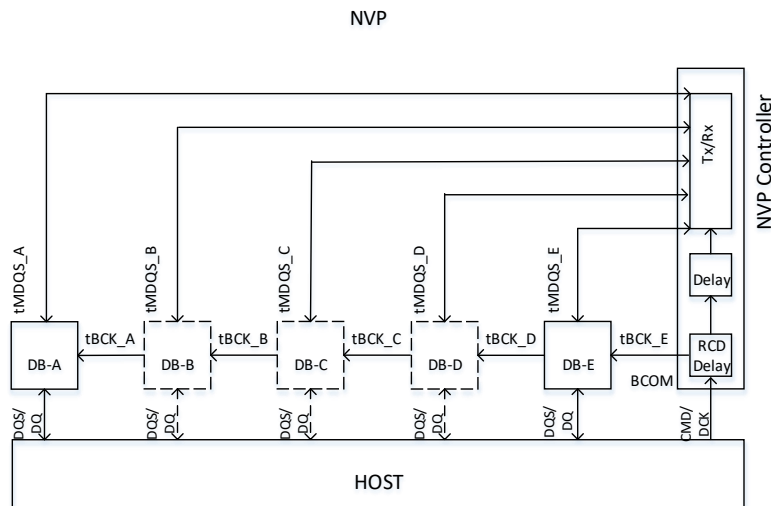


Figure 20 - Delay added for Data Buffer DB-A

Separate Programmable Command Delay MCWs are defined for read and write. The Read command delay is defined in MCW F3RC00 and the write command delay is defined in MCW F3RC01.

5.13 DQ Training

Similar to DQ training in DDR4 SDRAM based LRDIMM. SEND and XWRITE commands are supported to train media controller of the DDR4 NVDIMM-P. To avoid data read/write in non-volatile memory media, the Training Guard Key(MR6 A13) must be enabled by 1. While the Training Guard key is enabled, XADR command shall not be issued after the following XWRITE command.

5.13.1 MPR Pattern Mode

This mode is already defined in DDR4 SDRAM specification. This mode is enabled by setting MR3 A2 = 'H'(MPR enable) and MR3 A1:0 =00b(MPR page 0). Commands supported in this mode are MRS, SEND, XWRITE and DES. BA[1:0] pins for SEND and XWRITE command are used to address MPR location within MPR page 0. The NVDIMM-P must be in idle state only. Power-down mode is not allowed during MPR Pattern Mode.

MPR pattern mode, training patterns are sent to all DQ and check bit (CB) pins. All 72 DQ and CB pins toggle based on training patterns. ECC and messages in metadata normally sent by NVDIMM-P media controller are disabled under MPR Pattern mode.

For MPR reads, most of the requirements are identical to those in DDR4 SDRAM specification. The minimum gap between SEND commands for back-to-back reads from Page 0 is tCCD. In the command truth table for the SEND command, A0~A2 are assigned as zeros since data burst order is assumed to be in the fixed mode for the NVDIMM-P.

For MPR read format by SEND command, for serial, parallel, and staggered mode the read formats are identical to those defined in DDR4 SDRAM specification, where the formats apply to all 72 DQ and CB pins. For parallel and staggered data return mode, read from MPR page 1, MPR page 2, and MPR page 3 are not allowed.

For MPR write by XWRITE command, ADDR[30:23], the addresses that are assigned to A7~A0 pins, are assigned as data for MPR. ADDR-[30:23] will be input to the NVDIMM-P starting from the MSB to LSB (i.e., ADDR[30] at UI #0, ADDR-[23] at UI #7). XADR command shall not be issued after the following XWRITE command.

5.13.2 Advanced FIFO Training Mode

Advanced FIFO training mode is enabled by setting MR6 A8. Commands supported in this mode are MRS, SEND, XWRITE, and DES. The definition of the SEND command is identical to that defined in the MPR Pattern Mode. In this mode, a FIFO in the media controller is used for write/read DQ training.

Minimum FIFO depth is defined as 128 command entry in order to guarantee a complex back to back data pattern can be generated during training. XWRITE commands are used to write the requests in the media controller buffer, and SEND commands are used to read the request from the media controller buffer in FIFO (i.e., in-order) manner. After NVDIMM-P receives the XWRITE data, the data will be automatically stored in the read buffer instead of the NVDIMM-P memory media. After tFIFO time from the prior write data transfer, the SEND command shall be issued. Write credit does not apply for any write training. Once the SEND command is issued, one write buffer entry will be free. The subsequent XADR command shall not be issued after the following XWRITE command. The minimum gap between back-to-back XWRITE commands is 4 clocks.

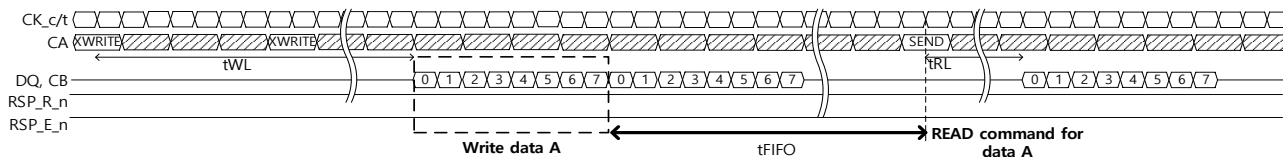


Figure 21 - Advanced FIFO Training Example

Under Advanced FIFO training mode, training patterns are sent to all DQ and check bit (CB) pins. All 72 DQ and CB pins toggle based on training patterns. ECC and messages in metadata normally sent by NVDIMM-P media controller are disabled under Advanced FIFO training mode.

5.13.3 Data Buffer Training

Steps for training data buffers and NVDIMM-P controller using these two modes are as follows:

- **DB MDQ Receive Enable Phase Training Mode (MREP)** – HOST enables MDQS Receive Enable Training mode in BC0C and MPR mode in NVP controller
 - HOST sends a sequence of SEND commands to NVP controller
 - HOST programs F0BC2x and F0BC3x for changing the MDQS delay until HOST finds the first rising edge of MDQS_t
 - The DB sampling circuit output is available on the DQ pins.
 - HOST program the final value by applying an offset to the training result (including F0BCCx)
- **NVP Controller to DB Read Delay Training Mode (MRD)** – HOST enables MRD in BC0C and MPR mode in NVP controller
 - HOST programs F0BC4x, F0BC5x for changing the MDQS_{x_t}/MDQS_{x_c} delay
 - HOST programs F4BC8x, F4BC9x, F4BCAx, F4BCBx for changing MDQ read delay
 - BC08 does not need to program considering only RANK0 is supported
 - The DB data pattern comparator output is available on the DQ pins. A logic one is driven when a match is found.
 - Host programs expected data patterns which are stored in F5BC0x, F5BC1x, F5BC2x, F5BC3x, F6BC0x, F6BC1x, F6BC2x, F6BC3x
 - MPR0[7:0] contains the expected first UI(UI0) for MDQ[7:0] while MPR7[7:0] contains the expected last UI(UI7) for MDQ[7:0]. Meaning MPRx[7:0] should match UIx for MDQ[7:0]
 - HOST issues SEND commands to NVP controller

- NVP Controller to DB Write Delay Training Mode (MWD) – HOST enables MWD in BC0C and Advanced FIFO training mode in NVP controller
 - Host programs data patterns which are stored in F5BC0x, F5BC1x, F5BC2x, F5BC3x, F6BC0x, F6BC1x, F6BC2x, F6BC3x
 - HOST programs F0BC8x, F0BC9x for changing MDQ-MDQS delay
 - HOST programs F4BCCx, F4BCDx, F4BCEx, F4BCFx for changing MDQ read delay
 - BC08 does not need to program considering only RANK0 is supported
 - Host issues XWRITE commands and data from these writes come from the DB MPRs
 - MPRx[7:0] is driven to UIx of MDQ[7:0] e.g., MPRx[7:0] is driven to MDQ[7:0]
 - HOST issues SEND commands
 - DB performs a bit wise comparison with data in the MPRs
 - DB comparator output is available on the DQ pins. A logic one is driven when a match is found.
 - DB training states can be seen from F6BC5x and its status can be controlled by F6BC4x

5.14 Unsupported DDR functions

The DDR4 functions listed below are not supported in DDR4 NVDIMM-P media controller.

- 2N Mode
- Data Mask(DM), Data Bus Inversion (DBI) and TDQS
- CAL Mode (CS_n to Command Address Latency)
- Control Gear Down Mode
- Additive latency
- Write CRC
- Per DRAM Addressability

6. Functional Features

6.1 Read/Write buffer management

6.1.1 Read buffer management

The Maximum Read Credit parameter is defined by NVDIMM-P module as the maximum number of concurrent 64-byte read transactions data that the module can accept. Maximum Read Credit is advertised in the NVDIMM SPD. Read transactions are defined as XREAD commands, including READ_STATUS (XREAD with RID=FFh) and SREAD commands.

The Maximum Read Credit can be read to manage and limit the number of read-data requests at a 64B granularity to the NVDIMM-P module. If the Maximum Read Credit is reached, the NVDIMM-P is not required to accept any further read commands until one or more previous read transactions complete. Completion occurs when data is transferred to the host after a SEND command or when data is transferred with an SREAD hit.

The Maximum Read Credit parameter does not limit the number of RIDs available for use.

In one example implementation, during power-up sequence or reset, host reads the Maximum Read Credit in SPD and initializes a Read Credit (RC) counter variable. RC counter is used to limit the number of outstanding read requests to the NVDIMM-P module. The host can issue a read transaction to the NVDIMM-P module as long as the RC counter is greater than zero. The host can decrement the RC counter by one with each read transaction issued to the NVDIMM-P module. When RC counter reaches a value of zero, the host stops issuing read transactions to NVDIMM-P module. The host will increment the RC counter only after successful completion of a read transaction, occurring when the data is received at the host after a SEND command or with an SREAD hit.

6.1.2 Write buffer management

The NVDIMM-P supports write buffers for posting XWRITES and PWRITES.

Upon initialization, the total available WC and PWC values can be accessed by READ_STATUS command (See 4.6.2, “

Available Credit Synchronization). The WC value represents the shared write buffer space in NVDIMM-P for XWRITE and PWRITE data at a 64-bytes granularity (e.g., 1 WC represents 64-bytes of buffer space). The PWC is independent of WC and the value represents the special entry space for PWRITE. For example the PWC may represent available energy backed buffer space for energy backed NVDIMM-P or available write grouping information register entry number when the write group option is supported. Therefore the number of XWRITES is limited by WC, and the number of PWRITES is limited by both PWC and WC. NVDIMM-P can report a value of PWC that is larger, smaller or equal to WC.

The NVDIMM-P returns credits to the host controller as space becomes available in write buffers. The NVDIMM-P provides write credit feedback to the host controller in response to a SEND command, using the WC[2:0] or CTH fields of the read data and message packet. The write credit from the NVDIMM-P indicates the number of newly available write buffer spaces (1 write credit is 64 bytes) since the last write credit feedback. Separate write credits are returned for XWRITES and PWRITES.

XWRITE and PWRITE buffering and buffer management are the responsibility of the NVDIMM-P. These buffers are primarily for the NVDIMM-P media controller to manage write traffic to the media which is the eventual destination of all XWRITES and PWRITES. The media controller is expected to manage such buffers for optimal write performance, not to rely on any other explicit command such as FLUSH or PWRITE with Persist =1 to drain XWRITE or PWRITE data from these buffers. Media controllers are expected to drain these buffers and return credits as space becomes available.

The available write credits on the NVDIMM-P dynamically changes as follows:

- XWRITE issued: WC decreased by 1
- PWRITE issued: WC decreased by 1 and PWC decreased by 1
- Shared Buffer released: WC increased by number of credits released
Released WC value presented in read data or message packet
- PWRITE buffer released: PWC increased by number of credits released
Released PWC value presented in read data or message packet

The NVDIMM-P can receive XWRITES if the available WC > 0

The NVDIMM-P can receive PWRITES if the available WC > 0 and the available PWC > 0

Three example implementations of data buffering on the NVDIMM-P are shown in Figure 22.

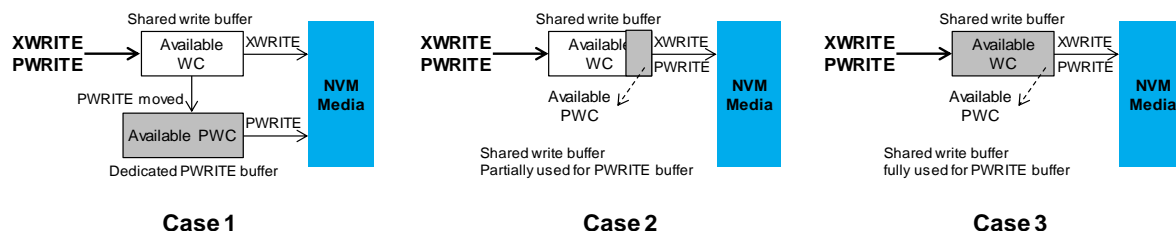


Figure 22 - Write buffer implementations

Examples of write credit availability:

Case 1: The initial credit values, defined in the message packet and available during initialization, are WC=8 and PWC=12. This represents Case 1 from Figure 22 - Write buffer **implementations**

Table 117 - Example of Case 1

Event	WC RETURN	PWC RETURN	Available WC	Available PWC
Initial credit values	-	-	8	12
XWRITE_1 issued	-	-	7	12
XWRITE_2 issued	-	-	6	12
XWRITE_3 issued	-	-	5	12
XWRITE_4 issued	-	-	4	12
XWRITE_5 issued	-	-	3	12
XWRITE_3 retired and credits returned	1	0	4	12
XWRITE_4 retired and credits returned	1	0	5	12
XWRITE_1 and XWRITE_5 retired and credits returned	2	0	7	12
PWRITE_1 issued	-	-	6	11
PWRITE_1 moved from shared to dedicated buffer	1	0	7	11
PWRITE_1 retired and credits returned	0	1	7	12

Case 2: The initial credit values, defined in the message packet and available during initialization, are WC=8 and PWC=4. This represents Case 2 from Figure 22 - Write buffer **implementations**

Table 118. Example of Case 2

Event	WC RETURN	PWC RETURN	Available WC	Available PWC
Initial credit values	-	-	8	4
XWRITE_1 issued	-	-	7	4
XWRITE_2 issued	-	-	6	4
XWRITE_3 issued	-	-	5	4
XWRITE_4 issued	-	-	4	4
XWRITE_5 issued	-	-	3	4
XWRITE_3 retired and credits returned	1	0	4	4
XWRITE_4 retired and credits returned	1	0	5	4
XWRITE_1 and XWRITE_5 retired and credits returned	2	0	7	4
PWRITE_1 issued	-	-	6	3
PWRITE_1 retired and credits returned	1	1	7	4

6.2 All-Zeros Fail-Prevention Mode

A codeword of all zeros is valid in the ECC scheme (See section 9, “

Channel Error Correction Code (ECC)”). In order to prevent the interface failure of all-zeros escaping the ECC, a mode to salt the check-bits is included. The mode can be enabled or disabled by F2RC4x bit. Once this mode is enabled:

- **Transmission of check-bits**
Each 8-bit check symbol shall be XORed with 8'hFFh post ECC check-bit coding on transmission. The XOR only applies to the check symbols CSn(m).
- **Reception of check-bits**
Each 8-bit check symbol shall be XORed with 8'hFF pre ECC check-bit decoding on reception. The XOR only applies to the check symbols CSn(m).

6.3 Write Data grouping

Write Data grouping(or Write Group ID) capability option is advertised in the NVDIMM SPD. If the “Write Group” is supported, the NVDIMM-P uses the WGID field to group multiple PWRITE commands. Similar to the read operation, the persistent write operation additionally includes an 8-bit transaction ID, the Write Group ID (WGID), to identify the specific group to which the persistent write data will be associated. Flush operations can target a specific WGID, with two flush scenarios supported by the NVDIMM to push a WGID set to NVM:

1. **Explicit FLUSH** : The host issues FLUSH[10] with a WGID command explicitly to instruct NVDIMM to transfer all write data associated with a given WGID group to NVM.
2. **Implicit FLUSH** : The host issues PWRITE command with the “persist” bit set (HIGH or logic-level 1) to instruct NVDIMM-P to transfer all write data associated with a given WGID group to NVM following the receipt of the last 64B chunk. Issuing this command operates the same as a PWRITE with ‘persist’ bit clear (LOW or logic-level 0) followed by FLUSH[10].

Multiple group flush request (such as FLUSH[10] or PWRITE with persist=1) with different WGIDs may be sent to the NVDIMM-P before the prior group flush completes.

After the NVDIMM-P successfully moves the data to NVM, the NVDIMM will trigger a W_PER response to the host. The retiring of data to NVM may be processed out of order, with the WGID bitmap indicating which flush request completed. The NVDIMM-P will assert the bit corresponding to the relevant WGID in the WGID bitmap when the data for the flush operation is persisted in NVM. The NVDIMM-P will transfer the WGID bitmap after receiving a MR-CT-WGID and SEND-MRR command.

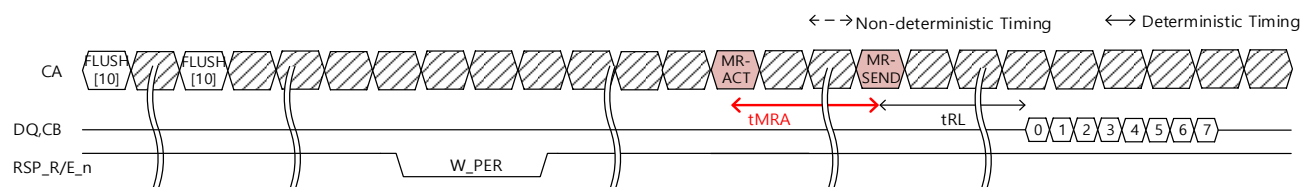


Figure 23 - MR-CT-WGID and SEND-MRR timing

Table 119 - WGID bitmap format

	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	WGID0	WGID1	WGID2	WGID3	WGID4	WGID5	WGID6	WGID7

DQ1	WGID8	WGID9	WGID10	WGID11	WGID12	WGID13	WGID14	WGID15
...
DQ31	WGID24 8	WGID24 9	WGID25 0	WGID25 1	WGID25 2	WGID25 3	WGID25 4	WGID25 5
DQ32	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
...
DQ63	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
CB0~ 5	ECC				ECC			
CB6	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
CB7	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

In the bitmap, each WGID bit position value represents the write group's status. At power up the WGID bitmap is initialized to all 1's. NVDIMM upon receiving a PWRITE with a new WGID will change status of the relevant WGID bit to '0'. Once all data associated with a given WGID has been written to the NVM then the corresponding bit is marked as '1'.

Nomenclature: PWRITE[0] : PWRITE with persist bit '0'.
PWRITE[1] : PWRITE with persist bit '1'

Figure 24 - WGID bitmap status **flow**, shows an example of ‘WGID bitmap’ flow control between Host and NVDIMM-P.

- 1) PWRITE[0] received with WGID=0. NVDIMM-P clears the WGID bit 0 to ‘0’.
- 2) PWRITE[0] received with WGID=1. NVDIMM-P clears the WGID bit 1 to ‘0’.
- 3) PWRITE[1] or FLUSH[10] received with WGID=0.
- 4) PWRITE[1] or FLUSH[10] received with WGID=1.
- 5) NVDIMM retires all data to NVM for WGID=1 and then asserts W_PER. Out of order retiring is allowed and illustrated in this example. NVDIMM sets WGID bit 1 to ‘1’ in ‘WGID bitmap’.
- 6) NVDIMM retires all data to NVM for WGID=0 and then asserts W_PER. NVDIMM sets WGID bit0 to ‘1’ in ‘WGID bitmap’.
- 7) NVDIMM receives a MRACT-WGID and SEND_MRR command. This command is valid after one or more W_PER responses have been transmitted since the last SEND_MRR sequence.
- 8) NVDIMM sends a ‘WGID bitmap’ with the WGID bit 0 and 1 set to ‘1’. The WGID bitmap must reflect the status of all PWRITE and FLUSH commands received by NVDIMM before MRACT-WGID and SEND_MRR commands. The WGID bitmap should also reflect status of all W_PERs asserted by NVDIMM before receiving MRACT-WGID and SEND_MRR commands.

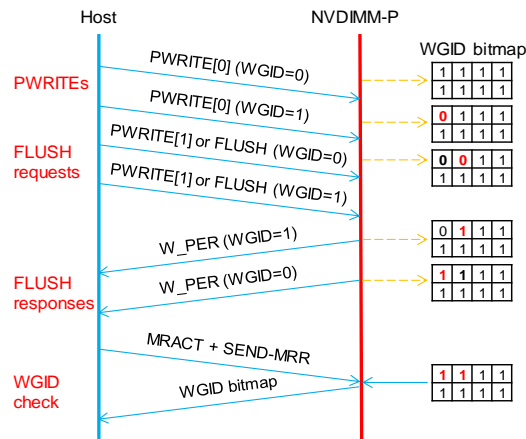


Figure 24 - WGID bitmap status flow

Multiple W_PER responses may be coalesced into one W_PER. Therefore, upon the completion of one or more writes in WGID bitmap, the NVDIMM-P may only send a single W_PER to the host, e.g., A host issues 3 PWRITE[1]s followed by FLUSH 01. Each of the three PWRITE[1]s and FLUSH[01] have a unique WGID. The NVDIMM may respond with a single W_PER upon completion of all flush requests. The WGID bitmap will reflect that the three PWRITE[1] commands and FLUSH[01] have been completed.

A PWRITE command that use the reserved WGID (FFh) cannot be grouped with other PWRITEs and is limited to a single 64B command. PWRITE commands using the reserved WGID (FFh) encoding, with persist=0, signify that completion response and WGID management is not required by the host controller, and therefore will not tracked by the NVDIMM.

Figure 25 shows an example of Channel Error Recovery using WGID bitmap.

If an UE (Uncorrectable Error) occurs when the WGID bitmap is transferred from the NVDIMM to the host controller, the transmitted WGID bitmap is not valid. However, the WGID bitmap on the NVDIMM is still correct and the host controller can request a new copy with a MRACT-WGID and SEND_MRR command. The NVDIMM can continue to receive PWRITE or FLUSH[10] commands after the transmission error, before receiving a request to resend the WGID bitmap. The WGID bitmap will be resent to the host controller after the NVDIMM receives a new MRACT-WGID and SEND_MRR request. The WGID bitmap will be prepared when the MRACT-WGID command is received, therefore reflecting the current, and potentially updated WGID state.

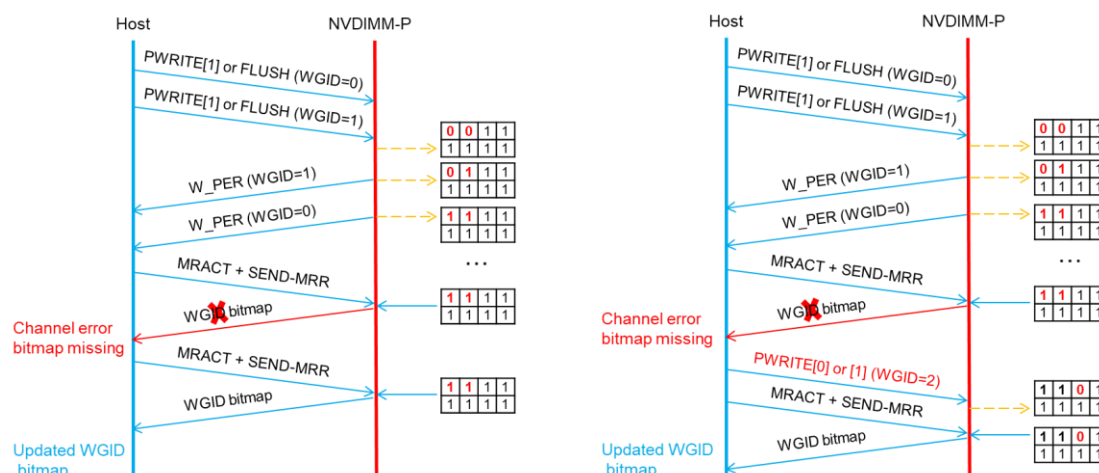


Figure 25 - WGID bitmap status flow with uncorrectable channel error

6.4 Data Persistence in the Event of a Power Loss

Writes to an NVDIMM-P are considered “persistent” once they are in a domain on the DIMM that can survive power loss at the system level. There are two approaches to ensuring this persistence before power-off and power fail:

- 1) **Power loss alert with Backup Energy:** In the power-on state, the write is persistent as soon as the DIMM moves it into these energy-backed buffers or caches. In the event of a system power loss, host issues the Final FLUSH command or performs a Catastrophic Save operation(defined in MMR specification), and there is a backup energy source that can provide the DIMM sufficient time to move writes in volatile buffers or caches to NVM media. The “ENERGY_SOURCE_POLICY” and “WRITE_DATA_POLICY ” register at Module Management Register (MMR) shall be set during the power-up initialization. Refer to the MMR(Modular Management Register) specification for more details.
- 2) **FLUSH completion response:** The host uses the FLUSH command, defined in section 4.5, “FLUSH” or an Implicit FLUSH operation defined in section 6.3, “Write Data grouping”, to move selected writes to NVM, with a completion response to the host when the data persistency is safely guaranteed in the NVDIMM-P. In the event of total power loss to the DIMM (including the loss of any backup energy source that may be present), any writes that are still in volatile buffers or caches on the DIMM will be lost.

The host shall use the PWRITE command for writes that require persistence. The DIMM may use this to select the buffers or caches that need to be moved to NVM media to survive power loss. The DIMM may also move XWRITES to NVM media during normal operation, but these are not required to survive system power loss.

The energy backing source may be at the DIMM level or the System level.

If the DIMM has its own backup energy source, the energy source is fully managed by the DIMM and reported to the host. Alternatively, in the case of DIMM which requires the system-based energy and the host has system-based backup energy source, the host shall program the system-based backup energy capability to the DIMM during boot time. Refer to the MMR(Modular Management Register) specification for more details.

Backup energy and Final FLUSH modes

The host will use the available (Host managed or Device managed) backup-energy information and the required backup energy information from the DIMM to determine which volatile content to flush in the event of a power loss as well as the cache write policy that the DIMM should use. The DIMM shall provide the ‘*Required-CS-Energy A~D*’ for each of the different write policies: Write-Through (WT) and/or Write-Back (WB). Host shall program the ENERGY_SOURCE_POLICY and WRITE_DATA_POLICY registers during boot time. The programmed backup energy source must be guarantee by the host, after system power loss. The table below describes the various cases of host-selected write policy and the Final FLUSH mode which can be used by the host.

- *Required-CS-Energy A* to save the WT(Write Through) mode PWRITE data
- *Required-CS-Energy B* to save the WB(Write Back) mode PWRITE data
- *Required-CS-Energy C* to save the WT(Write Through) mode PWRITE and XWRITE data
- *Required-CS-Energy D* to save the WB(Write Back) mode PWRITE and XWRITE data

Table 120 - Final Flush Modes

Available Energy (from System and DIMM)	DIMM Write Policy (Programmed by Host)		Final FLUSH Modes on Power Loss
	PWRITE	XWRITE	
< Required-CS-Energy-A	WB	WB	N/A
>= Required-CS-Energy-A	WT	WB	01 (PWRITE)
>= Required-CS-Energy-B	WB	WB	01 (PWRITE)
>= Required-CS-Energy-C	WT	WT	00 (ALL)
>= Required-CS-Energy-D	WB	WB	00 (ALL)

NOTE 1 In the case of ‘Self-managed energy backed DIMM (Required-CS-Energy Backup_Energy_A~D=FFh)’, the DIMM supplies all the required backup energy, therefore all Final FLUSH modes can be allowed by the host regardless of any other backup energy condition or write policy setting.

7. Error and Event Alert

7.1 Error type

7.1.1 CA parity error

The NVDIMM-P device shall employ the same scheme for command/address bus parity as defined by the DDR4 RCD specification.

Refer to the “*JESD82-31, DDR4 Registering Clock Driver – DDR4RCD01 Specification, 2.4 Parity*”

To recover from this error scenario, refer to the 7.2, “Error handling and recovery”

Error Case	Response signal	Message packet(RID=FFh)	Error Log
C/A Parity Error	PAR_ERR (by ALERT_n)	N	F0RCC~F0RCF

7.1.2 Read Channel error

The channel ECC defined in Section 9, “

Channel Error Correction Code (ECC)” verifies the transmission of the read data packet or message packet returned from the NVDIMM-P. If an uncorrectable error (UE) on read data is detected as a result of SEND command, the data and metadata transferred from the NVDIMM-P is compromised. The specific read that failed cannot be identified since the RID returned may be invalid. Additionally, the credit response field (WC[2:0]) cannot be guaranteed and therefore is invalid. To recover from this error scenario, refer to the section 7.2, “Error handling and recovery”.

Multiple SEND commands could be issued before an UE is detected on one of the read data packets. It is left to the Host to determine which reads are to be retried following the reset.

7.1.3 Write Channel error

When an uncorrectable channel ECC error on write data packet is detected in the NVDIMM-P, the NVDIMM-P shall employ the same ALERT_n scheme for write CRC error as defined by the DDR4 specification. Due to the different ECC implementation than DDR4 SDRAM, tWECC_ALERT may be longer than DDR4 SDRAM. The NVDIMM-P SPD provides the NVDIMM-P required tWECC_ALERT value.

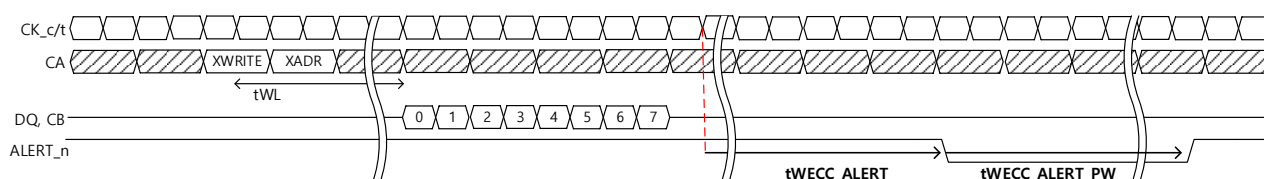


Figure 26 - Write channel ECC Error Reporting

The error address with VALID=1, TYPE[3:0]=0001b and STATUS[7:0]=FFh are logged in MWC F4RC8x~F4RCE_x Event Log register.

Refer to the “*JESD79-4B, DDR4 SDRAM Specification, 4.16 CRC*”.

To recover from this error scenario, refer to the 7.2, “Error handling and recovery”.

Error Case	Response signal	Message packet(RID=FFh)	Error Log
Write Channel error	WECC_ERR (by ALERT _n)	N	F4RC8x~F4RCE _x

7.1.4 UE response of read request

If the NVDIMM-P detects an Uncorrectable media error on the read requested address, it shall generate a UE response message (message packet with POISON=1, ERID=RID of request with error, VALID_ERR=1 and , UE=1) instead of a read data packet. Returning the UE response message indicates that the valid read-data packet corresponding the ERID cannot be returned because of an uncorrectable media error detected on the requested address. So if the host receives the UE response message, the host shall complete the read-request in data error state and release the corresponding RID. The purpose of UE response message is the Error RID delivery for the host to clear read-requests. To avoid a missing Error address upon a channel error on the UE response message packet, the error address with VALID=1, TYPE[3:0]=0001b and STATUS[7:0]=FEh is logged in MWC F4RC8x~F4RCE_x Event Log register

Error Case	Response signal	Message packet(RID=FFh)	Error Log
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Uncorrectable media Error for read request	RD_RDY (by RSP_R_n)	POISON=1, VALID_ERR=1 and UE=1 ERID = Error RID	F4RC8x~F4RCEx
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7.1.5 Interrupt

The NVDIMM-P generates an interrupt message packet when internal errors or warning events (such as correctable channel error, wear-out and etc.) are detected. The message packet includes INT_TYPE and INT_ADDR with VALID_INT=1 and the interrupt information is logged in the Event Log register (F4RC8x~F4RCEx). The register can be overwritten by multiple other events, so it is recommended to clear the Event Log register in the interrupt handling process. Unlike the URGENT event, the interrupt message does not indicate a media controller, or protocol error. Therefore, normal operation will continue even if the interrupt message is transferred. For correctable channel errors, the host has the option to enable and disable the interrupt and to set an error threshold after which the NVDIMM-P will stop reporting interrupts via MCW F2RC5x.

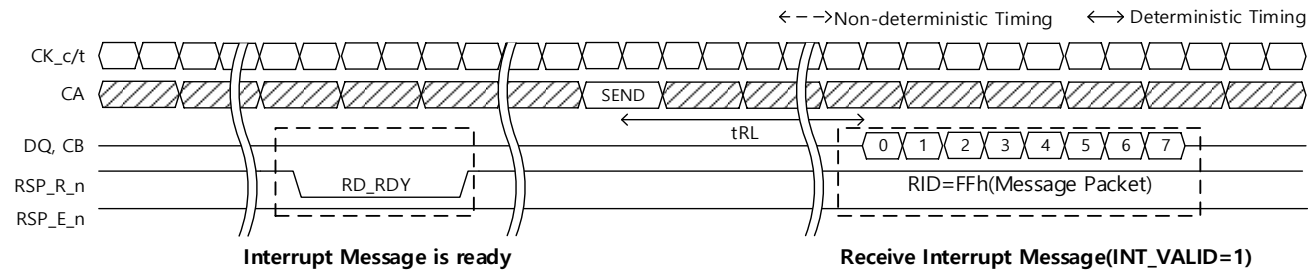


Figure 27 - NVDMM-P Interrupt message operation

Table 121 describes the interrupt types supported by the NVDIMM-P.

- ✓ Write Data Link Corrected ECC Error: returned upon a corrected ECC on Write
- ✓ Temperature above Threshold: returned based on detection of over-temp threshold. Note; interrupt for over temp threshold may be generated in conjunction with Temp Above Threshold Error.
- ✓ Unconsumed Uncorrectable Error Detected
- ✓ SMART / Health Trip
- ✓ SEND Overflow: Returned in the case in which a SEND command is received by a response packet is not available (no corresponding RD_RDY returned by the NVDIMM).
- ✓ Write Error with Buffered Data: NVDIMM detected an error writing data to persistent media, however data is still retained in buffers for READs.

Table 121 - Interrupt type

Interrupt type	INT_TYPE[3:0]
NONE	0000b
ERROR	0001b
WARNING	0010b
Others	Others

Table 122 - Interrupt Status

Interrupt Status	ADDR_VALID	INT_STATUS[7:0]
Write Data Link Corrected ECC Error	1	00h
Temperature Above Threshold	0	01h
Unconsumed Uncorrectable Error Detected	1	02h
SMART / Health Trip	0	03h
SEND Overflow	0	04h
Write Error with Buffered Data	0	05h
Reserved	others	06h

7.1.6 Urgent error

Urgent errors, errors typically resulting in lost data and requiring immediate response by the host controller, fall under the following categories:

- Write Error : examples include result of a WC overflow, or PWC overflow
- Read Error : examples include duplicate RID.
- Controller Error: examples include a fatal error, or thermal shutdown error

For these errors which are signaled to the host controller via the urgent response mechanism, a log shall be provided by the NVDIMM-P for debug purposes. MCW Function Space 2 is used to store the urgent error log (F2RCCx~F2RCFx). The Error Log is cleared following a RESET_n LOW signal and individual error log bits are cleared by host MRS to the respective MCW. A read-only version of the log shall also be provided through the module management registers.

Error Case	Response signal	Message packet(RID=FFh)	Error Log
Urgent Error	URGENT (by RSP_R_n)	N	F2RCx~F2RFx

7.1.7 Data persistency error in the event of a Power Loss

Refer to the MMR(Modular Management Register) specification for more details

7.2 Error handling and recovery

1) Read Channel error recovery.

- ① Host issues the READ_STATUS[11] (RESET_RID) to NVDIMM-P (See section 4.6.3, “Reset RID”).
- ② NVDIMM-P asserts RD_RDY response signal when the RESET_RID operation is completed.
- ③ Host issues the SEND command to get a message packet which include RID_RDY =1 with VALID_RDY indicating that no pending reads exists in the NVDIMM-P.
- ④ Host issues the READ_STATUS[01] (Write Credit sync) to NVDIMM-P (See 4.6.2, “

- ⑤ **Available Credit Synchronization**”).
 - ⑥ NVDIMM-P asserts RD_RDY when the message packet includes Available WC and PWC is ready.
 - ⑦ Host issues the SEND command to get a message packet which includes VALID_WC and VALID_PWC bits are 1.
 - ⑧ Host updates its WC and PWC counter.
 - ⑨ Host reads the F4RC8x~F4RCEx register to determine whether the error packet was message packet or not.
 - ⑩ If INT=1 in F4RC8x, Host should process the interrupt handling action.
 - ⑪ NVDIMM-P is ready to receive read requests including reissue of discarded requests.
- 2) Write Channel error recovery.
- ① Host rewrites the error data if it is possible.
 - ② Host issues the READ_STATUS[01] (Write Credit sync) to NVDIMM-P (See 4.6.2, “

- ③ **Available Credit Synchronization**).
- ④ NVDIMM-P asserts RD_RDY when the message packet includes Available WC and PWC is ready.
- ⑤ Host issues the SEND command to get a message packet which includes VALID_WC and VALID_PWC bits are 1.

3) CA Parity error recovery.

Refer to the “*JESD82-31 DDR4 Registering Clock Driver – DDR4RCD01 Specification, Section 2.4 Parity*”

Host rewrites the all prior data if it is possible and process “Read data channel error recovery” to ensure a precise NVDIMM-P state that is consistent with the host controller.

7.3 Error Injection

For the purposes of debug and testing of an NVDIMM-P device it is useful to provide control and read-out for various types of errors which may occur via the NVDIMM-P host interface. Error types for which error injection is provided regardless of address are described as follows:

- Host channel write and read ECC, correctable and uncorrectable
- Host channel read user metadata error
- Host channel CA parity
- RID timeout
- Write credit overflow
- SEND overflow
- Controller fatal error
- Other, vendor-specific cases, as required

Additionally, error injection for an Uncorrectable ECC error at a single, specified target address is provided. For this case, the host writes any number of times after armed (this avoids issues whereby a CPU cache flush overwrites the address with good data). Once armed, the first read to the specified address returns an Uncorrectable ECC error, and disarms further injection. Subsequent reads to the target address return “good” status.

Injection control for all of these errors may be either timer-based, or one-shot instances. Once armed, the NVDIMM-P shall inject an error on next host request that meets the trigger criteria.

Error injection registers are provided by MCW F2RC7x through F2FCBx. The host issues MRS commands to set UECC address or error injection mask bit(s). Multiple error injection mask bits may be set for timer-based error types. The NVDIMM-P controller arms a single error when the timer expires. The timer is restarted after the injected error is triggered. The NVDIMM controller subsequently selects the next enabled error. To enable error injection the host issues an MRS to F2RC6x:DA[7]=1. One-shot and UECC address error types shall self-clear upon a trigger. For timer-based error types the host issues an MRS command to F2RC6x:DA[7]=0 to clear the enable.

Error injection for error types which are signaled and/or logged separately via the sideband interface are provided for as part of the module management registers.

8. Power Management

8.1 Power-up and Reset initialization

For power-up and reset initialization, in order to prevent NVDIMM-P media controller from functioning improperly, default values for the following MR settings are defined.

- Clock-Stopped Power Down Mode (MR4 A[0]) : 0 = Disable
- CS to Command/Address Latency (MR4 A[8:6]) : 000 = Disable
- CA Parity Latency Mode (Media Control Word) : F0RC0E DA[0]=0(Disable)

8.1.1 Power-up initialization

1. Apply power (RESET_n is recommended to be maintained below $0.2 \times VDD$; all other inputs may be undefined). RESET_n needs to be maintained below $0.2 \times VDD$ for minimum time (t_{INIT}) with stable power. CKE is pulled “Low” any time before RESET_n being de-asserted (min. time $10ns$ ~~t_{ACT}~~). The power voltage ramp between 300mV to VDD min must be no greater than 200ms; and during the ramp, $VDD \geq VDDQ$ and $(VDD - VDDQ) < 0.3$ volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times. In addition:
 - All input receivers are disabled, and may be left floating.
 - Since internally generated Vref is selected in F0RC0B DA3 (see DDR4 RCD Specification) for Input Receiver Vref source after RESET_n is driven LOW, the reference voltage (VrefCA) does not need to be stable
 - All control registers are restored to their default states, which is all ‘0’s unless explicitly stated otherwise
 - As long as the RESET_n input is pulled LOW, the register is in low power state and input termination is not present and all response pins are not driven.
2. After RESET_n is de-asserted, wait for another 1 ms before activating CKE. During this time, the media in the NVDIMM-P will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK_t, CK_c) need to be started and stabilized for at least t_{STAB} and the DLL locked, before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (t_{IS}) must be met. Also a Deselect command must be registered (with t_{IS} set up time to clock) at clock edge Td. Once the CKE registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of t_{DLLK} and t_{ZQinit} . Also, RSP_R/E_n signals are driven HIGH after t_{ACT} .
4. The NVDIMM-P media controller keeps its on-die termination in high-impedance state as long as RESET_n is asserted. Furthermore, the NVDIMM-P controller keeps its on-die termination in high impedance state after RESET_n de-assertion until CKE is registered high. The ODT input signal may be in undefined state until t_{IS} before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. The ODT input signal must be statically held LOW if RTT_NOM is to be enabled in buffer control word (BCW). In all cases, the ODT input signal remains static until the power-up initialization sequence is finished, including the expiration of t_{DLLK} and t_{ZQinit} .
5. After CKE is registered high, wait minimum of Reset CKE Exit time, t_{XPR} , before issuing the first MRS command to load mode register. ($t_{XPR} = \text{Max}(t_{XS}, 5nCK)$)

6. Issue MRS Command to load MR7 with all media controller control word settings (To issue MRS command to MR7, provide “High” to BG0, BA1, BA0).
7. Issue MRS Command to load MR6 with all application settings (To issue MRS command to MR6, provide “Low” to BA0, “High” to BG0, BA1). Internal media training bit (MR6 A[9]) must be set to 1 for media training start. Once MR6 A[9] is set, internal media training will be performed. Therefore after this step, when MR6 register is programmed again, MR6 A[9] shall be programmed 0 as NOP(No Operation) to avoid a multiple internal media training start.
8. Issue MRS Command to load MR3 with all application settings (To issue MRS command to MR3, provide “Low” to BG0, “High” to BA1, BA0).
9. Issue MRS Command to load MR5 with all application settings (To issue MRS command to MR5, provide “Low” to BA1, “High” to BG0, BA0).
10. Issue MRS Command to load MR4 with all application settings (To issue MRS command to MR4, provide “Low” to BA1, BA0, “High” to BG0)
11. Issue MRS Command to load MR2 with all application settings (To issue MRS command to MR2, provide “Low” to BG0, BA0, “High” to BA1)
12. Issue MRS Command to load MR1 with all application settings (To issue MRS command to MR1, provide “Low” to BG0, BA1, “High” to BA0)
13. Issue MRS Command to load MR0 with all application settings (To issue MRS command to MR0, provide “Low” to BG0, BA1, BA0)
14. Issue MRS Command to load MR7 with all data buffer control word settings (To issue MRS Command to MR7, provide “High” to BG0, BA1, BA0).
15. Issue ZQCL command to start ZQ calibration.
16. Wait for t_{ZQ} init completed.
17. Issue MRS Command to MR6 A[13]= 1 to enable the “Training Guard key”
- 18.** Perform the read/write training (including Vref and Write Leveling). See 5.1.3, “

19. DQ Training”.

20. Issue MRS Command to MR6 A[13]= 0 to disable the “Training Guard key”

21. Issue READ_STATUS[00] (Addr[3:2]=00b). If RD_RDY is asserted, issue a SEND command until the RDY_PWR=1 (NVDIMM-P controller initialization is completed). After the “Training Guard key” is disabled, any normal read/write operation such as XWRITE/PWRITE and XREAD shall not be issued before the RDY_PWR is set to 1. The ready status can be checked by I2C bus in MCW F2RC03-DA[1] register alternately.

A NVDIMM-P power-up sequence is shown in Figure 28, “NVDIMM-P Power-up Sequence”.

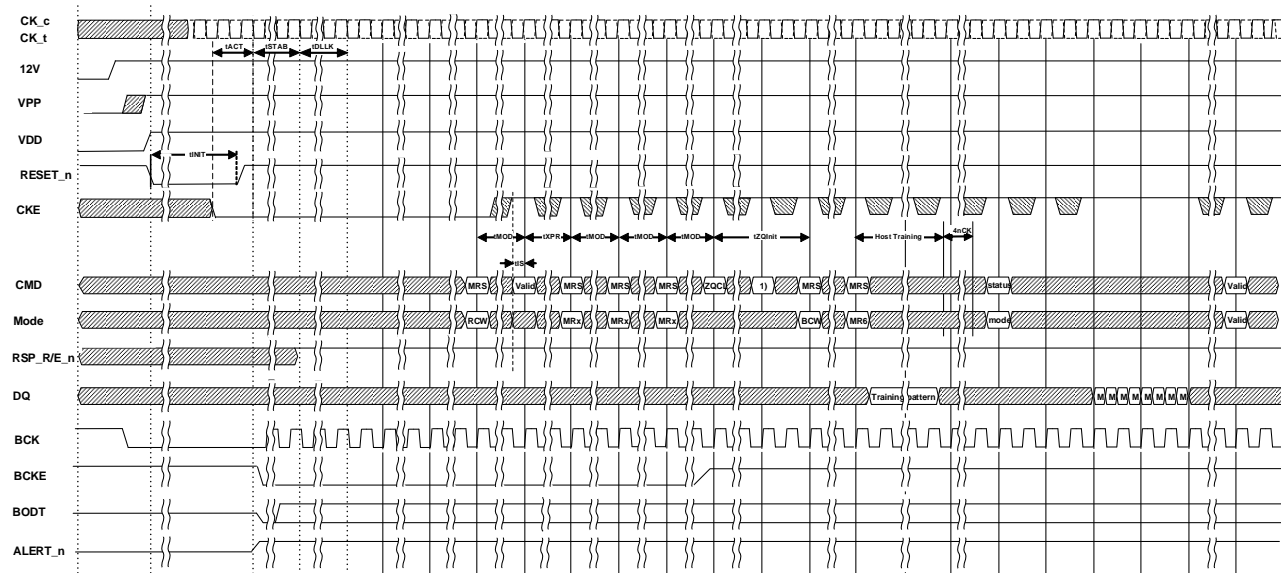


Figure 28 - NVDIMM-P Power-up Sequence

8.1.2 Reset initialization

Refer to the “*JESD79-4B, DDR4 SDRAM Specification, 3.3 Reset Initialization Procedure*”.

tPW_RESET time is different from DDR4 SDRAM

8.2 Power saving mode

The DDR4 NVDIMM-P provides multiple methods of support for power saving modes. Both the DDR4 Power Down Mode (clock stopped as well as non-clock stopped) entry and exit as well as Self-Refresh entry and exit operations are supported to enable DIMM power savings as well as system power savings through clock frequency changes. The following sections describe the power saving mode entry and exit operations, timing parameters, requirements, and DIMM functionality for these modes.

8.2.1 Non-clock Stopped Power-down

The DLL or PLL should be in a locked state when power-down is entered for fastest power-down exit timing.

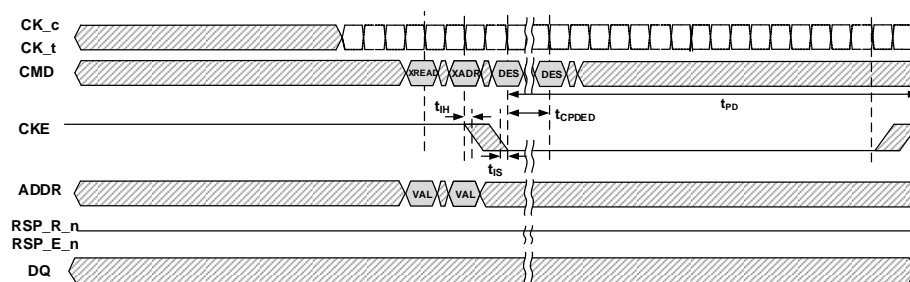


Figure 29 - NVDIMM-P Power-Down Entry

Power-down entry (PDE), as illustrated in Figure 29, “NVDIMM-P Power-Down Entry”, can be issued from the idle state or from the active state. If any requests for data and metadata reads, writes, and flushes issued before PDE issue are pending, then the NVDIMM-P will enter the power-down mode after all in-progress commands are completed. For any read or persistent write requests that wait for response signals, the response signals operate as normally defined in the active mode, using either RSP_R_n or RSP_E_n signals. Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, CS_n, RSP_R_n, RSP_E_n and RESET_n. In power-down mode, NVDIMM-P ODT input buffer is deactivated based on mode register MR5 bit A5. If the bit is set to 0, ODT input buffer remains activated and ODT input signal must be at valid logic level. If the bit is set to 1, ODT input buffer is deactivated, the NVDIMM-P ODT input signal is not driven (i.e., floating) and the NVDIMM-P media controller does not provide RTT_NOM termination. Termination information such as RTT_NOM and RTT_PARK is available in the Buffer Control Word (BCW) instead of MRs.

Also, the DLL is kept enabled during power-down. In power-down mode, CKE low, RESET_n high, and a stable clock signal must be maintained at the inputs of the DDR4 NVDIMM-P for time t_{STAB} , and ODT should be in a valid state, but all other input signals are “Don’t Care”. If in any case RESET_n goes low, then the NVDIMM-P will exit power-down mode and enter the reset state. During the power-down mode, multiple Deselect commands are needed during the CKE switch off and cycle(s) after to protect internal delay on CKE line to block the input signals. This timing period for issuing multiple Deselect commands is defined as tCPDED. CKE=Low will result in deactivation of command and address receivers after tCPDED has expired.

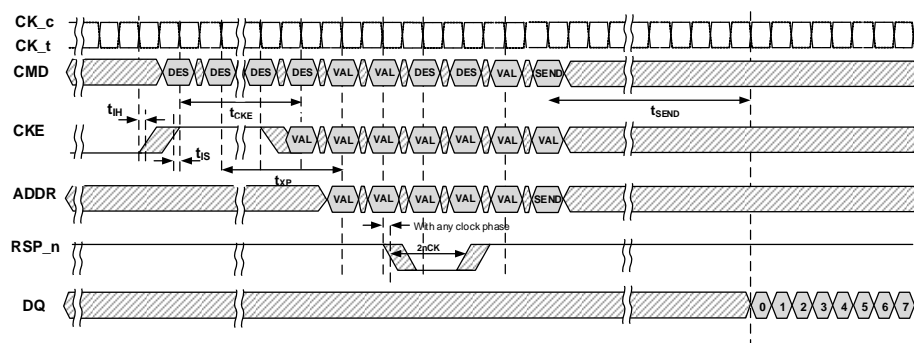


Figure 30 - NVDIMM-P CKE Power-Down Exit with Response Signal & SEND Examples

As illustrated in Figure 30, “NVDIMM-P CKE Power-Down Exit with Response Signal & SEND Examples”, the power-down state is synchronously exited when CKE is registered high (along with a Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP after CKE goes high, where tXP is defined as

deterministic timing from the power-down exit issue to the timing when the NVDIMM-P is ready to proceed to the active state. The t_{XP} value for the NVDIMM-P power-down will be defined in SPD that covers power-down exit latencies. It is possible that the NVDIMM-P media controller may trigger response signal to the host before t_{XP} timing.

Different levels of power-down modes may exist in the NVDIMM-P, depending on the media types adopted by the NVDIMM-P. At some level only the media controller is in the power-down state, or the volatile memory media attached to the NVDIMM-P are in the power-down state. For power-down states other than the default state defined, MRS command is used to enter power-down states and power-down exit (PDX) command is used to exit from those states.

8.2.2 Clock Stopped Power-down

To support any operations that allow output clocks to float, the Clock Stopped Power-down Mode is supported for the NVDIMM-P. For stopping the clock, procedures described in the Clock Stopped Power-down Mode in the DDR4 RCD Specification are used, where DLL/PLL can also be powered off.

In order to support all existing features supported in DDR4 RCDs, Clock Stopped Power-down Mode is entered with MRS command, where MR4 A0 is used to enable Clock Stopped Power-down Mode. Detailed procedures are illustrated in Figure 31, “MRs Use in Clock Stopped Power-Down Entry”.

All power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VPP, and VREFCA) must be at valid levels.

In contrast to the Non-clock stopped power-down mode, for any read or persistent write requests that wait for response signal, the response signal will be activated after the power-down mode is exited since the NVDIMM-P cannot return response via RSP_R or RSP_E signals in Clock Stopped Power-down Mode. And the time out counter value for each read and persistent write requests will be suspended during the power down time.

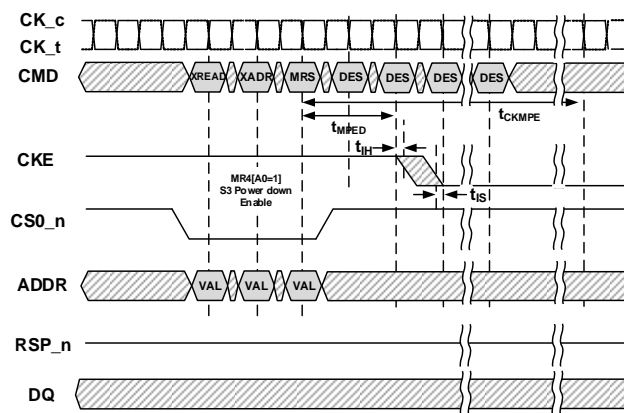


Figure 31 - MRs Use in Clock Stopped Power-Down Entry

In order to exit the Clock Stopped Power-down Mode, first CS0_n must be driven to HIGH (to prevent accidental access to the control registers), and CKE must be driven to LOW. After that, a frequency and phase accurate input clock signal must be applied. Then, PDX command is used where CS0_n signal is at valid LOW level and LOW-to- HIGH CKE transition is detected. Since clock receivers are not active during this time, CS_n = ‘LOW’ is captured by detecting the rising edge of the CKE signal. Figure 32, “Clock Stopped Power-Down Exit with Response Signal & SEND Examples”, describes how the Clock Stopped Power-down Mode exit is executed with the subsequent example of response signal applied from the NVDIMM-P, which allows SEND command issue.

Similar to the Non-clock stopped power-down mode, t_{XP} is defined in SPD. Furthermore, t_{XP_DLL} is also defined in SPD. During the exit time t_{XP} , only DES commands are allowed. During the exit time t_{XP_DLL} , SEND or SREAD requiring a locked DLL/PLL is not allowed. After the power-down exit is applied, the NVDIMM-P media controller clears the MR4 A0 bit to 0 to disable this mode.

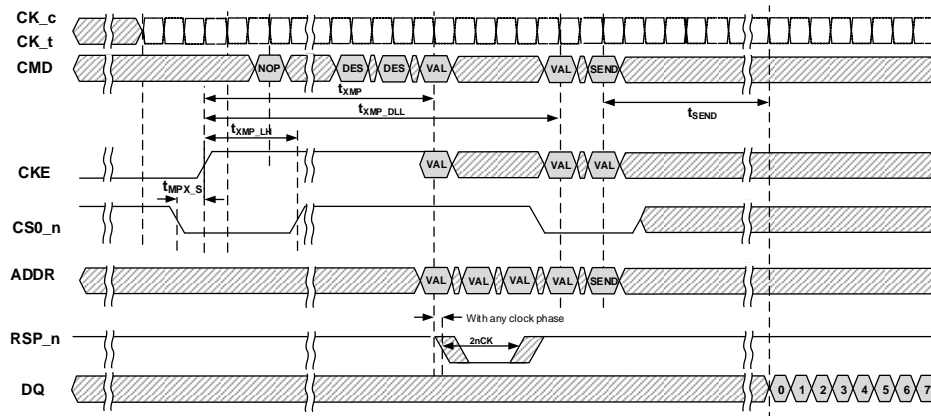


Figure 32 - Clock Stopped Power-Down Exit with Response Signal & SEND Examples

8.2.3 Self-Refresh

The DDR4 NVDIMM-P Self-Refresh operation is used to support either or both changes to the NVDIMM-P input clock frequency as well as reduced power standby modes. The Self-Refresh-Entry (SRE) Command is defined by having CS_n, RAS_n/A16, CAS_n/ A15, and CKE held low with WE_n/A14 and ACT_n high at the rising edge of the clock.

By default, the NVDIMM-P shall support clock frequency changes, P0 mode. The NVDIMM-P may support up to three low-power modes (P1-P3) each providing additional power-savings. For each subsequent power-mode the self-refresh exit time and response timings may increase. Because the power savings will be media-dependent, actual power savings and exit timings for each mode are vendor-specific. The low-power standby modes supported by the NVDIMM-P, and their attributes, are discoverable by SPD.

The mode enabled/disabled by the SRE/SRX command is pre-programmed by an MRS command to the MWC F2RC3x. Programmed mode settings not supported by a particular NVDIMM will be ignored by the NVDIMM and the default P0 mode will be used.

When entering Self-Refresh Operation to support only an input clock frequency change (mode P0), all outstanding data burst operations as well as calibration operations must be complete and the NVDIMM should be in an idle state (no pending read request and write buffer empty by returning all write credit).

When entering Self-Refresh Operation to support system power-management modes, before issuing the Self-Refresh-Entry command, all pending XREAD operations shall be completed and data persistency shall be ensured by a FLUSH operation.

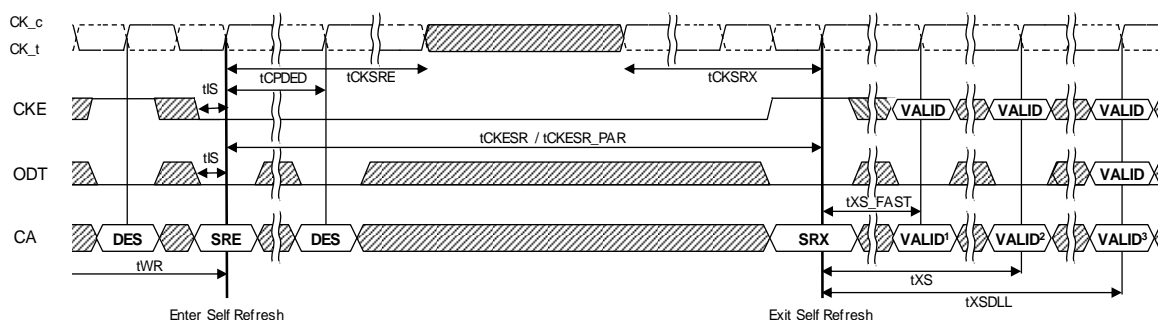
During the self-refresh operation, the NVDIMM-P does not return RD_RDY nor W_PER responses via the RSP_R_n and RSP_E_n signals. URGENT response signals may still be issued by the NVDIMM, but are dependent upon which low-power mode is selected.

Following the Self-Refresh-Entry (SRE) command, the operation of the NVDIMM-P follows the DDR4 SDRAM Self-Refresh operation sequence. Refer to the “*JESD79-4B DDR4 SDRAM Specification, Section 4.27 Self Refresh Operation*”

Table 123 - Self-Refresh mode

Mode	Exit Timing until Commands Decoded	Time Until Full Performance	Support of Response (RD_RDY, URGENT)	Notes
P0	t_{XS} / t_{XSDLL}	0	Y	CFC only; No low power state
P1	t_{XS} / t_{XSDLL}	Min	Y	Reduced power state; increased XREAD response time until full performance
P2	t_{XS} / t_{XSDLL}	Mid	N	Further reduced power; increased XREAD response time until full performance
P3	t_{XS} / t_{XSDLL}	Max	N	Max power savings; increased XREAD response time until full performance

The exit timing from Self-Refresh exit to first valid command not requiring a locked DLL is t_{XS} . The value of t_{XS} is 10ns.



NOTE:

1. Only MRS (limited to those described in the Self-Refresh Operation section). ZQCS or ZQCL command allowed.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.

Figure 33 - Self-Refresh Entry/Exit Timing

9. Channel Error Correction Code (ECC)

The channel ECC provides protection for the data and transaction information only. Data protection for the volatile and non-volatile media on the NVDIMM-P device is provided by the on-board media controller. DDR4 NVDIMM-P devices employ a Reed Solomon code with 8 bit symbols. Each BL8 transaction contains two code words and each code word is comprised of four UI's or 288 bits. The ECC Reed Solomon Symbol Correction Code is defined as {36, 33} with 8-bit symbols. There are 36 symbols with 33 symbols used for Data+Metadata and 3 symbols for ECC.

The parameters for this code are:

- $M = \text{bits per Symbol} = 8$
- $N = \text{Number of Symbols in Code Word} = 288/M = 36$
- $K = \text{Number of Symbols in Message (Data + Metadata)} = 264/M = 33$

The NVDIMM-P ECC provides error detection/correction as follows:

- Single Symbol Correction:
 - 2 adjacent lane failures or transient bursts correct up to 8 bit errors
- Double Symbol Detection–100%
 - Any 2 8-bit symbol errors per code-word
 - Max 16-bit and min 2-bit burst error detection

9.1.1 Data Mapping

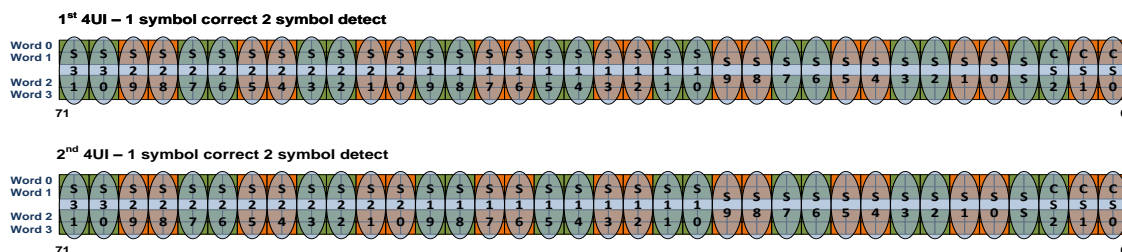


Figure 34 - NVDIMM-P ECC Data Mapping

This section covers the parameters and mapping of the channel as a whole, denoting the Data Symbols (DS0-DS31), the Metadata Special Symbol (SS) and the Common Check Symbols (CS0-CS2). The data mapping for NVDIMM-P ECC is shown in following table. Each 8UIs memory transaction contains 2 code words, each of which contains 288 bits over 4UIs.

Table 124 - NVDIMM-P ECC Data Mapping

Connector Pin	UI0	UI1	UI2	UI3	Connector Pin	UI0	UI1	UI2	UI3
CB0	CS0(0)	CS0(2)	CS0(4)	CS0(6)	DQ28	DS14(0)	DS14(2)	DS14(4)	DS14(6)
CB1	CS0(1)	CS0(3)	CS0(5)	CS0(7)	DQ29	DS14(1)	DS14(3)	DS14(5)	DS14(7)
CB2	CS1(0)	CS1(2)	CS1(4)	CS1(6)	DQ30	DS15(0)	DS15(2)	DS15(4)	DS15(6)
CB3	CS1(1)	CS1(3)	CS1(5)	CS1(7)	DQ31	DS15(1)	DS15(3)	DS15(5)	DS15(7)
CB4	CS2(0)	CS2(2)	CS2(4)	CS2(6)	DQ32	DS16(0)	DS16(2)	DS16(4)	DS16(6)
CB5	CS2(1)	CS2(3)	CS2(5)	CS2(7)	DQ33	DS16(1)	DS16(3)	DS16(5)	DS16(7)
CB6	SS0(0)	SS0(2)	SS0(4)	SS0(6)	DQ34	DS17(0)	DS17(2)	DS17(4)	DS17(6)
CB7	SS0(1)	SS0(3)	SS0(5)	SS0(7)	DQ35	DS17(1)	DS17(3)	DS17(5)	DS17(7)
DQ0	DS0(0)	DS0(2)	DS0(4)	DS0(6)	DQ36	DS18(0)	DS18(2)	DS18(4)	DS18(6)
DQ1	DS0(1)	DS0(3)	DS0(5)	DS0(7)	DQ37	DS18(1)	DS18(3)	DS18(5)	DS18(7)
DQ2	DS1(0)	DS1(2)	DS1(4)	DS1(6)	DQ38	DS19(0)	DS19(2)	DS19(4)	DS19(6)
DQ3	DS1(1)	DS1(3)	DS1(5)	DS1(7)	DQ39	DS19(1)	DS19(3)	DS19(5)	DS19(7)
DQ4	DS2(0)	DS2(2)	DS2(4)	DS2(6)	DQ40	DS20(0)	DS20(2)	DS20(4)	DS20(6)
DQ5	DS2(1)	DS2(3)	DS2(5)	DS2(7)	DQ41	DS20(1)	DS20(3)	DS20(5)	DS20(7)
DQ6	DS3(0)	DS3(2)	DS3(4)	DS3(6)	DQ42	DS21(0)	DS21(2)	DS21(4)	DS21(6)
DQ7	DS3(1)	DS3(3)	DS3(5)	DS3(7)	DQ43	DS21(1)	DS21(3)	DS21(5)	DS21(7)
DQ8	DS4(0)	DS4(2)	DS4(4)	DS4(6)	DQ44	DS22(0)	DS22(2)	DS22(4)	DS22(6)
DQ9	DS4(1)	DS4(3)	DS4(5)	DS4(7)	DQ45	DS22(1)	DS22(3)	DS22(5)	DS22(7)
DQ10	DS5(0)	DS5(2)	DS5(4)	DS5(6)	DQ46	DS23(0)	DS23(2)	DS23(4)	DS23(6)
DQ11	DS5(1)	DS5(3)	DS5(5)	DS5(7)	DQ47	DS23(1)	DS23(3)	DS23(5)	DS23(7)
DQ12	DS6(0)	DS6(2)	DS6(4)	DS6(6)	DQ48	DS24(0)	DS24(2)	DS24(4)	DS24(6)
DQ13	DS6(1)	DS6(3)	DS6(5)	DS6(7)	DQ49	DS24(1)	DS24(3)	DS24(5)	DS24(7)
DQ14	DS7(0)	DS7(2)	DS7(4)	DS7(6)	DQ50	DS25(0)	DS25(2)	DS25(4)	DS25(6)
DQ15	DS7(1)	DS7(3)	DS7(5)	DS7(7)	DQ51	DS25(1)	DS25(3)	DS25(5)	DS25(7)
DQ16	DS8(0)	DS8(2)	DS8(4)	DS8(6)	DQ52	DS26(0)	DS26(2)	DS26(4)	DS26(6)
DQ17	DS8(1)	DS8(3)	DS8(5)	DS8(7)	DQ53	DS26(1)	DS26(3)	DS26(5)	DS26(7)
DQ18	DS9(0)	DS9(2)	DS9(4)	DS9(6)	DQ54	DS27(0)	DS27(2)	DS27(4)	DS27(6)
DQ19	DS9(1)	DS9(3)	DS9(5)	DS9(7)	DQ55	DS27(1)	DS27(3)	DS27(5)	DS27(7)
DQ20	DS10(0)	DS10(2)	DS10(4)	DS10(6)	DQ56	DS28(0)	DS28(2)	DS28(4)	DS28(6)
DQ21	DS10(1)	DS10(3)	DS10(5)	DS10(7)	DQ57	DS28(1)	DS28(3)	DS28(5)	DS28(7)
DQ22	DS11(0)	DS11(2)	DS11(4)	DS11(6)	DQ58	DS29(0)	DS29(2)	DS29(4)	DS29(6)
DQ23	DS11(1)	DS11(3)	DS11(5)	DS11(7)	DQ59	DS29(1)	DS29(3)	DS29(5)	DS29(7)
DQ24	DS12(0)	DS12(2)	DS12(4)	DS12(6)	DQ60	DS30(0)	DS30(2)	DS30(4)	DS30(6)
DQ25	DS12(1)	DS12(3)	DS12(5)	DS12(7)	DQ61	DS30(1)	DS30(3)	DS30(5)	DS30(7)
DQ26	DS13(0)	DS13(2)	DS13(4)	DS13(6)	DQ62	DS31(0)	DS31(2)	DS31(4)	DS31(6)
DQ27	DS13(1)	DS13(3)	DS13(5)	DS13(7)	DQ63	DS31(1)	DS31(3)	DS31(5)	DS31(7)

9.1.2 Field Definition

The field used to define the code is GF(256). For mapping the elements of the field to a bit-level representation, the elements are defined as GF(2) polynomials modulo the primitive GF(2) polynomial $x^8 + x^4 + x^3 + x^2 + 1$. This definition is repeated below:

Table 125 - Primitive Polynomial Matrix

Alpha Power	Binary value	Alpha Power	Binary value	Alpha Power	Binary value	Alpha Power	Binary value	Alpha Power	Binary value	Alpha Power	Binary value	Alpha Power	Binary value
0	1	38	10010100	76	111110	114	111110	152	1001001	190	10101110	228	111101
1	10	39	110101	77	111100	115	1111100	153	10010010	191	1000001	229	1111010
2	100	40	1101010	78	1111000	116	11111000	154	111001	192	10000010	230	11110100
3	1000	41	11010100	79	11110000	117	11101101	155	1110010	193	11001	231	11110101
4	10000	42	10110101	80	11111101	118	11000111	156	11100100	194	110010	232	11110111
5	100000	43	1110111	81	11100111	119	10010011	157	11010101	195	1100100	233	11110011
6	1000000	44	11101110	82	11010011	120	111011	158	10110111	196	11001000	234	11111011
7	10000000	45	11000001	83	10111011	121	1110110	159	1110011	197	10001101	235	11101011
8	11101	46	10011111	84	1101011	122	11101100	160	11100110	198	111	236	11001011
9	111010	47	100011	85	11010110	123	11000101	161	11010001	199	1110	237	10001011
10	1110100	48	1000110	86	10110001	124	10010111	162	10111111	200	11100	238	1011
11	11101000	49	10001100	87	1111111	125	110011	163	1100011	201	111000	239	10110
12	11001101	50	101	88	11111110	126	1100110	164	11000110	202	1110000	240	101100
13	10000111	51	1010	89	11100001	127	11001100	165	10010001	203	11100000	241	1011000
14	10011	52	10100	90	11011111	128	10000101	166	11111	204	11011101	242	10110000
15	100110	53	101000	91	10100011	129	10111	167	111110	205	10100111	243	1111101
16	1001100	54	1010000	92	1011011	130	101110	168	11111100	206	1010011	244	11111010
17	10011000	55	10100000	93	10110110	131	1011100	169	11100101	207	10100110	245	11101001
18	101101	56	1011101	94	1110001	132	10111000	170	11010111	208	1010001	246	11001111
19	1011010	57	10111010	95	11100010	133	1101101	171	10110011	209	10100010	247	10000011
20	10110100	58	1101001	96	11011001	134	11011010	172	1111011	210	1011001	248	11011
21	1110101	59	11010010	97	10101111	135	10101001	173	11110110	211	10110010	249	110110
22	11101010	60	10111001	98	1000011	136	1001111	174	11110001	212	1111001	250	1101100
23	11001001	61	1101111	99	10000110	137	10011110	175	11111111	213	11110010	251	11011000
24	10001111	62	11011110	100	10001	138	100001	176	11100011	214	11111001	252	10101101
25	11	63	10100001	101	100010	139	1000010	177	11011011	215	11101111	253	1000111
26	110	64	1011111	102	1000100	140	10000100	178	10101011	216	11000011	254	10001110
27	1100	65	10111110	103	10001000	141	10101	179	1001011	217	10011011		
28	11000	66	1100001	104	1101	142	101010	180	10010110	218	101011		
29	110000	67	11000010	105	11010	143	1010100	181	110001	219	1010110		
30	1100000	68	10011001	106	110100	144	10101000	182	1100010	220	10101100		
31	11000000	69	101111	107	1101000	145	1001101	183	11000100	221	1000101		
32	10011101	70	1011110	108	11010000	146	10011010	184	10010101	222	10001010		
33	100111	71	10111100	109	10111101	147	101001	185	110111	223	1001		
34	1001110	72	1100101	110	1100111	148	1010010	186	1101110	224	10010		
35	10011100	73	11001010	111	11001110	149	10100100	187	11011100	225	100100		
36	100101	74	10001001	112	10000001	150	1010101	188	10100101	226	1001000		
37	1001010	75	1111	113	11111	151	10101010	189	1010111	227	10010000		

9.1.3 Generator Polynomial

Generator polynomial is represented below

$$\text{Generator} = (x + \alpha^0)(x + \alpha^1)(x + \alpha^2) = x^3 + \alpha^{198} * x^2 + \alpha^{199} * x + \alpha^3$$

Table 126 - Generator Polynomial Matrix (Hex values)

	S 31	S 30	S 29	S 28	S 27	S 26	S 25	S 24	S 23	S 22	S 21	S 20	S 19	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 09	S 08	S 07	S 06	S 05	S 04	S 03	S 02	S 01	S 00	SS	CS 2	CS 1	CS 0	
S31	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B6	47	F0	
S30	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1E	EC	F3	
S29	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F4	E8	1D	
S28	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	20	14	35	
S27	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	25	DB	FF	
S26	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	7B	59	23	
S25	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EE	CB	24	
S24	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8A	7F	F4	
S23	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	90	5D	CC	
S22	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	97	52	C4	
S21	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	96	52	C5	
S20	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3B	37	0D	
S19	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	22	D5	F6	
S18	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D7	3D	EB	
S17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F7	28	DE	
S16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D2	F3	20	
S15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	04	CE	CB	
S14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F3	E7	15	
S13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	21	14	34	
S12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	88	BE	37	
S11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	62	BB	D8	
S10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1B	23	39	
S09	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	AA	6A	C1	
S08	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	B5	86	32	
S07	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	41	6F	2F	
S06	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	61	7B	1B	
S05	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	E9	C4	2C	
S04	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	8B	7F	F5	
S03	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3D	38	04	
S02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	8E	B0	3F	
S01	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	63	BA	D8	
S00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1B	22	38
S0S	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	07	0E	08

10. On-Die Termination

Refer to the “*JESD79-4B DDR4 SDRAM Specification, Section 5. On-Die Termination*”.

11. Absolute Maximum Ratings

Refer to the “*JESD79-4B DDR4 SDRAM Specification, Section 6. Absolute Maximum Ratings*”.

12. AC & DC Input/Output Measurement Levels

Refer to the “*JESD79-4B DDR4 SDRAM Specification, Section 8. AC & DC Input Measurement Levels*”.

Refer to the “*JESD79-4B DDR4 SDRAM Specification, Section 9. AC & DC Output Measurement Levels*”.

13. Speed Bin

Table 127 - Timing parameter

Timing Parameter		Value		Unit
Parameters	Symbol	min	max	
NVDIMM-P Timing				
FIFO turnaround time for Advanced FIFO training mode enable	tFIFO	SPD	-	nCK
RESET_RID init latency	tRESET_RID_INIT	SPD	-	nCK
RESET_RID timeout	tRESET_RID_MAX	-	SPD	ns
Command and Address Timing				
CAS_n to CAS_n command delay for MPR disable mode	tCCD	4	-	nCK
DLL locking time	tDLLK	See Table 128		nCK
Write data Recovery Time (Write to Read or Flush command delay to same address)	tWR	SPD	-	nCK
Read(XREAD/SREAD) to Write(XWRITE/PWRTIE) command delay to same address	tWAR	SPD	-	nCK
Mode Register Set command cycle time	tMRD	8	-	nCK
Control word to control word delay Number of clock cycles between an access to F0RC03, F0RC04, F0RC05, F0RC0BDA0 and F0RC7x and the next control word access	tMRD_L	48	-	
Control word to control word delay Number of clock cycles between an access to F0RC0F & F0RC0D and the next control word access or NVDIMM-P command	tMRD_L2	48	-	

Mode Register Set command update delay	tMOD	48	-	nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD(min)+AL+PL	-	nCK
Clock Stopped Power Down Timing				
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	
Valid clock requirement before MPSM exit	tCKMPX	max(5nCK, 10ns)	-	
Exit MPSM to commands not requiring a locked DLL	tXMP	10	-	ns
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tDLLK(min)	-	
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	
Calibration Timing				
Power-up and RESET calibration time	tZQinit	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	nCK
Power Up / Reset Timing				
Power Up Initialization time	tINIT	4	-	ms
Inputs active time before RESET_n de-assertion	tACT	Max(16nCK, 10ns)	-	nCK
Clock stabilization time	tSTAB	5	-	uS
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, 10ns)	-	nCK
Valid Clock Requirement before Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	nCK
Self-Refresh Timing				
Exit Self-Refresh to commands not requiring a locked DLL	tXS	10	-	ns
Exit Self-Refresh to ZQCL, ZQCS and MRS(CL, CWL, tWR and DLL Reset)	tXS_FAST	10	-	ns
Exit Self-Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK
Minimum CKE low width for Self-Refresh entry to exit timing	tCKESR	tCKE(min) + 1nCK	-	nCK
Minimum CKE low width for Self-Refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min) + 1nCK + PL	-	nCK
Valid Clock Requirement after Self-Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	nCK

Valid Clock Requirement after Self-Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max(5nCK, 10ns) + PL	-	nCK
Valid Clock Requirement before Self-Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	nCK
Power Down Timing				
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK, 6ns)	-	nCK
CKE minimum pulse width	tCKE	max(3nCK, 5ns)	-	nCK
Command pass disable delay	tCPDED	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	-	nCK
Timing of SEND command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry	tWRPDEN	WL+4	-	nCK
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	3	nCK
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	See Table 128		
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	See Table 128		
Write ECC Error Reporting				
Write ECC error to ALERT_n latency	tWECC_ALERT	3	SPD	ns
Write ECC ALERT_n pulse width	tWECC_ALERT_PW	6	10	nCK
Clock Timing	Refer to the DDR4 specification			
Data Strobe Timing	Refer to the DDR4 specification			
ODT Timing	Refer to the DDR4 specification			
Write Leveling Timing	Refer to the DDR4 specification			

NOTE MRD or SPD in the Value column indicate that the specification is media-dependent, and provided via either a mode register or SPD register which must be read upon NVDIMM-P initialization.

Table 128 - Timing parameter by Speed Grade

	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit
Symbol	min	max	min	max	min	max	min	max	min	max	min	max	min	max	
tDLLK	597	-	597	-	768	-	768	-	854	-	940	-	1024	-	nCK
tPAR_ALERT_PW	48	96	56	112	64	128	72	144	80	160	88	176	96	192	nCK
tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	-	71	-	78	-	85	nCK

14. Input/Output Capacitance

Same as DDR4 SDRAM

Refer to the “*JESD79-4B DDR4 SDRAM Specification, Section 12. Input/Output Capacitance*”.

15. Electrical Characteristics and AC Timing

Same as DDR4 SDRAM

Refer to the “*JESD79-4B DDR4 SDRAM Specification, Section 13. Electrical characteristics and AC Timing*”.

Annex A Profile

A.1 Commands

Command	Description	Profile 0	Profile 1
MRS	Mode Register Set	Y	Y
XADR	Extended Address	Y	Y
XWRITE	Transaction Write	Y	Y
PWRITE	Transaction Write with Persistence	Y	N
XREAD	Transaction Read	Y	Y
SREAD	Speculative Read	Y	N
SEND	Send read or message packet	Y	Y
SEND-MRR	Send Mode-register packet	Y	N
UNMAP	Unmap	Y	N
FLUSH	Flush	Y	N
NOP	No Operation	Y	Y
DES	Deselect	Y	Y
PDE	Power Down Entry	Y	Y
PDX	Power Down Exit	Y	Y
SRE	Self-Refresh Entry	Y	Y
SRX	Self-Refresh Exit	Y	Y
ZQCS	ZQ Calibration Short	Y	Y
ZQCL	ZQ Calibration Long	Y	Y

A.2 Functions

Function	Description	Profile 0	Profile 1
SAVE_n pin	Final Flush Operation	Y	Y
tRRSE	Latency Optimization	Y	Y
WAR ordering	Write after Read ordering	Y	N
Out-of-order transactions	Command queuing for performance optimization	Y	Y
Data Burst Ordering	32B reordering of 64B data burst	Y	N
Meta Burst Ordering	Reordering the RID and user-meta of meta-data burst	Y	Y
Metadata Option A	4 user metadata in read/write packet	Y	Y
Metadata Option B	6 user metadata in read/write packet	Y	Y
Write data Grouping	PWRITE Data Grouping and status bitmap report	Y	N
All Zeros Fail Prevention	To prevent the DQ failure of all-zeros data pattern	Y	Y
IOP0	Internal Operation Mode 0	Y	N
IOP1	Internal Operation Mode 1	Y	N

Annex B Module Management Features

B.1 Operations

This annex further describes the operations that the Host may request the module to perform and the Module Management Register (MMR) where module information, configuration and commands are accessed. While an operation is running on the module, the only operations that can be initiated are the Abort and Management operations. If the current running operation is the Abort operation, the only operation that can be initiated by the Host is the Management operation. If the Host attempts to initiate an operation that cannot be executed due to a current running operation, the module shall ignore the Host initiated operation.

B.1.1 Catastrophic Save Operation

The module shall support the Catastrophic Save operation. During the Catastrophic Save operation, the module shall move all data in volatile buffer and/or cache space into the non-volatile memory.

The module shall support the ability to initiate a Catastrophic Save operation through the START_SAVE bit in the NVDIMM_FUNC_CMD0 register in page 0 or the SAVE_N pin. The module shall also support ability to configure whether the SAVE_N pin low is driven low during the duration of the Catastrophic Save operation through the SAVE_N_LOW_DURING_CSAVE bit in the MODULE_OPS_CONFIG register in page 0.

Upon the start of the Catastrophic Save operation, the module shall set CSAVE_FAIL_INFO0 and CSAVE_FAIL_INFO1 registers to 0 and drive the SAVE_N pin low for the duration of the Catastrophic Save operation if the SAVE_N_LOW_DURING_CSAVE bit in the MODULE_OPS_CONFIG register is 1. Instead of the START_SAVE bit or SAVE_N pin, issuing FLUSH command with Final tag is another way to initiate a Catastrophic Save operation.

Upon completion of the Catastrophic Save operation, the module shall update the SAVE_STATUS0 and CSAVE_INFO1 registers in page 0, disable all triggers and unmask the RESET_N pin on the module. If a Catastrophic Save operation fails, the module shall persist information about the cause(s) of the Catastrophic Save operation failure in the CSAVE_FAIL_INFO0 and CSAVE_FAIL_INFO1 registers.

The host shall also initiate a Catastrophic Save operation in scenarios where a platform hard reset is needed. Examples of these scenarios include fatal platform errors such as NMI or host memory controller errors.

B.1.2 SAVE_N Pin

For modules supporting Catastrophic Save operation initiation through the SAVE_N pin, the module shall start the Catastrophic Save operation based on the SAVE_N pin as defined in Section B.1.1.

B.1.3 Erase Operation

Modules shall support the Erase operation. During the Erase operation, the module shall erase the **entire** non-volatile memory and set the NVM_Data_Valid bit in the CSAVE_INFO register in page 0 to 0. The Erase operation is initiated through the START_ERASE bit in the NVDIMM_FUNC_CMD0 register in page 0. Upon completion of the Erase operation, the module shall update the ERASE_STATUS0 register in page 0.

Three types of Erase Operation are supported:

- Block Erase(Default) : Erase the entire device,
- Overwrite(TBD) : Overwrite the entire device with host defined data pattern, and
- Crypto Erase(TBD) : Deletes the crypto key

B.1.4 Management Operations

Modules shall support Management Operations. Management Operations are operation that allow the Host to reset the controller on the module, command the module to not assert the EVENT_N pin or clear specific or all operation status registers on the module. Management operations are requested through the NVDIMM_MGT_CMD0 or NVDIMM_MGT_CMD1 register in page 0.

If the Host reset the controller on the module, the Host shall use the value of the NVDIMM_READY register to determine when initialization of the controller on the module is completed. When the controller has finished initialization, the module shall return the value 0xA5.

B.1.5 Set Energy Source Policy Operation

Modules may support the Set Energy Source Policy operation. During the Set Energy Source Policy operation, the module shall configure the Energy Source to use during the Catastrophic Save operation. If the module supports more than one Energy Source policy, it shall support the Set Energy Source Policy operation. A module can only be configured to one Energy Source policy.

B.1.6 Energy Source Policy

The module shall support at least one of the following Energy Source policies. A module may support both Energy Source policies.

- **Device Managed:** The module is responsible for monitoring the health of the Energy Source and ensuring there is sufficient energy to support a Catastrophic Save operation. The Energy Source used is either located on the module or tethered to the module. A tethered Energy Source may be dedicated to the module or shared between modules. The module shall not draw power from the 12V pin during a Catastrophic Save operation. A module that supports the Device Managed Policy shall support page 1.
- **Host Managed:** The Host is responsible for monitoring the health of the Energy Source and ensuring there is sufficient energy to support a Catastrophic Save operation. The Energy Source used is from the DIMM connector and may be dedicated to the module or shared between modules.

In Device Managed mode, the module shall communicate information about the Energy Source used. The Energy Source may be located on the module or tethered to the module.

B.1.7 Required CS(Catastrophic Save) Energy and Write data retire policy

The volatile content on the DIMM is required to be pushed to NVM media in the event of a power loss. This implies that all writes to be persisted have been issued by the host over NVDIMM-P interface and have been received without errors on the DIMM. In the event of a power loss the host may wish to flush either just PWRITES or both PWRITES and XWRITES. The Volatile content to be flushed to NVM media may be present in the following places on the DIMM:

- 1) Write-Buffers or Write Queues where incoming host writes are pending transfer
- 2) Optional DRAM or SRAM cache located on the DIMM

Depends on the write data retire policy and where the data is located, the CS energy requirement may be different. Therefore, the DIMM provides the CSAVE_POWER_REQ_A~D and CSAVE_TIMEOUT_A~D registers for each different backup-energy requirements. And depending on the total energy capability, the DIMM's write retire policies for PWRITE and XWRITE shall be set during the power-up initialization.

- A. Required CS Energy to save the WT(Write Through) mode PWRITE data
- B. Required CS Energy to save the WB(Write Back) mode PWRITE data
- C. Required CS Energy to save the WT(Write Through) mode PWRITE and XWRITE data
- D. Required CS Energy to save the WB(Write Back) mode PWRITE and XWRITE data

B.1.8 Set Event Notification Operation

Modules shall support the Set Event Notification operation. During the Set Event Notification operation, the module shall either enable or disable notification about specified events. When initiating the Set Event Notification operation, the Host specifies the event(s) for which notification shall be enabled or disabled through the SET_EVENT_NOTIFICATION_CMD register in page 0. Upon completion of the Set Event Notification operation, the module shall update the SET_EVENT_NOTIFICATION_STATUS0 register in page 0.

B.1.9 Firmware Operations

Modules shall support Firmware Operations. Firmware Operations are operations related to firmware update and consists of the following operations:

- Set Firmware Update mode
- Clear firmware data region
- Generate checksum for the firmware data region.
- Commit the firmware data region.
- Validate firmware header in the firmware data region.
- Validate the firmware image transferred to the module.

To update firmware, the Host shall first enable Firmware Update mode on the module. If a Host has not enabled Firmware Update mode on the module, the module shall fail all Firmware Operations except the Set Firmware Update mode operation. While the module is in Firmware Update mode, the module shall fail all other operations except the Abort operation.

To initiate a Firmware Operation, the Host shall set the appropriate bit in the FIRMWARE_OPS_CMD register in page 0. Upon completion of the Firmware operation, the module shall update the FIRMWARE_OPS_STATUS register in page 0.

B.1.10 Abort Operation

Modules shall support the Abort operation for the Catastrophic Save, Erase and Firmware Operations. In the Abort operation, the module shall stop the currently running Catastrophic Save, Erase and Firmware Operations. The Abort operation is initiated through the ABORT_CURRENT_OP bit in the NVDIMM_FUNC_CMD0 register in page 0. The Host should use the Abort operation if it detects that a pending operation has exceeded its worst case completion latency.

1) Abort a Catastrophic Save Operation

When a Catastrophic Save operation is aborted, the module shall not set the NVM_Data_Valid bit in the CSAVE_INFO register in page 0. The contents of buffer and/or cache space saved to non-volatile memory are indeterminate.

2) Abort Erase

When an Erase operation is aborted, module shall clear the NVM_Data_Valid bit in CSAVE_INFO register in page 0 if any data has been erased from non-volatile memory.

3) Abort Firmware Operations

The following Firmware Operations can be aborted.

- Clear firmware data region
- Generate firmware data region checksum
- Commit firmware data region
- Validate firmware image

When the clear firmware data region operation is aborted, the contents of the firmware data region is indeterminate.

When the generate firmware data region checksum operation is aborted, the contents of FW_REGION_CRC0 and FW_REGION_CRC1 registers shall not be change.

When the commit firmware data region operation is aborted, the contents of firmware slot 1 is indeterminate. SLOT1_FWREV0 and SLOT1_FWREV1 registers shall be set to 0 to indicate an invalid firmware is present.

B.1.11 Factory Default Operation

The module shall support a Factory Default operation which returns the module to the factory default state. When this command is initiated, the module shall

- Erase all data in the NVM except the data needed to determine warranty compliance.
- Disable all event notifications and enabled Catastrophic Save triggers.
- Clear the Energy Source policy on the module.
- Reset all readable registers to their default values except the registers needed to determine warranty compliance. The register descriptions in B.2 define which registers are not impacted by the Factory Default operation.

The Factory Default operation shall not affect the firmware on the module.

B.1.12 Energy Source

A NVDIMM-P may require an Energy Source to function correctly. This section describes the various Energy Source that may be supported by a module.

B.1.12.1 Local Energy Source

A local Energy Source is an Energy Source that is located on the module itself. A module uses the local Energy Source in Device Managed Policy.

B.1.12.2 Tethered Energy Source

A tethered Energy Source is an Energy Source that is connected to the module through a connector on the module. A module uses a tethered Energy Source in Device Managed Policy.

B.1.12.3 Host Energy Source

A host Energy Source is an Energy Source that is located on the Host. The energy from a Host Energy Source is provided to the module through the 12V pin. A module uses a host Energy Source in Host Managed Policy.

B.1.12.4 Shared Energy Source

A shared Energy Source is an Energy Source that is shared across multiple modules. Shared Energy Source may be used when the module is in either Device Managed Policy or Host Managed Policy.

B.1.13 Event Notification

A module may support asynchronous notification for events that require the Host's attention. Event notification is implemented through the EVENT_N pin on the DDR4 bus. An enabled event occurs when the value of the state changes (i.e., edge type event and not level type event). When an enabled event occurs, module shall drive the EVENT_N pin on the DDR4 bus to low until the corresponding event notification is disabled or the Host commands the module to not assert the EVENT_N pin.

If the module supports notification, the module shall support notification for persistency and warning threshold events. A module may support notification for vendor specific events.

When an event triggers, the Host shall do the following:

1. Set the DEASSERT_EVENT bit in NVDIMM_MGT_CMD1 to command the module to not assert the EVENT_N pin.
2. Read MODULE_HEALTH to determine the high level event source for the notification.
3. If event is caused by PERSISTENCY_LOST_ERROR, read MODULE_HEALTH_STATUS0, MODULE_HEALTH_STATUS1 and ERROR_THRESHOLD_STATUS registers for the specific cause of the PERSISTENCY_LOST_ERROR.
4. If event is caused by WARNING_THRESHOLD_EXCEEDED, read WARNING_THRESHOLD_STATUS to determine the warning threshold that caused the notification. If desired, readjust the warning threshold and enable event notification.
5. If event is caused by PERSISTENCY_RESTORED or BELOW_WARNING_THRESHOLD, this is to alert the Host that the previous error or warning condition is not present anymore. To determine the specific condition(s) that is not present, the Host reads either MODULE_HEALTH_STATUS0, MODULE_HEALTH_STATUS1 and ERROR_THRESHOLD_STATUS registers or WARNING_THRESHOLD_STATUS register.

B.1.14 Error and Warning Thresholds

Error thresholds allow the Host to know the warranty limits of the module. Warning thresholds allow the Host to get advance notification of when the module is reaching its warranty limit.

All threshold events shall be normalized to a range of 0 to 100% where 100% represents a good status. Module may support event notification if a value exceeds the threshold and if the value meets or fall below the previously exceeded threshold.

Warning thresholds shall have a default value set by the module manufacturer. Host shall be allowed to modify a warning threshold if it is supported. A warning threshold cannot conflict with an error threshold.

To set a warning threshold, the Host shall do the following:

1. Disable the event notification for the desired threshold.
2. Update the threshold value to the desired value.
3. Enable the event notification for the desired threshold.

B.1.15 Module Firmware

The module shall support 2 firmware images. There shall be a default image at firmware slot 0 that is flashed during manufacturing and not updatable afterwards. Modules shall support updating the firmware in slot 1 only if the Host enables firmware update mode. If the Host has not enabled firmware update mode on the module, the module shall fail all Firmware Operations.

The default image shall be a full functional image. To update the module firmware, see 1.B.2.4.

Firmware image shall begin with a 32-byte common header with the following format.

Table 129 - Firmware image header

Field Name	Byte Offset(s)	Description
Module Manufacturer ID	0 – 1	Module manufacturer ID. Shall match SPD bytes 320 – 321.
Module Product Identifier	2 – 3	Module product identifier. Shall match SPD bytes 192 – 193.
Vendor-Defined	4 – 19	Vendor defined 16 byte value.
Firmware Image Size	20 – 23	Size of the firmware image including the common header.
Firmware Image Checksum	24 – 25	CRC of the firmware image that does not include the common header. CRC is calculated using the CRC algorithm described in B.1.15.1.
Reserved	26 – 31	Reserved.

B.1.15.1 CRC Algorithm

The checksum in the firmware image header and in the FW_REGION_CRC0 and FW_REGION_CRC1 registers shall be calculated using the algorithm described in this section. This CRC algorithm is the same algorithm used to calculate the CRC fields in the SPD.

The following algorithm (shown in C) is to be followed in calculating and checking the code.

```
int Crc16 (char *ptr, int count)
{
    int crc, i;

    crc = 0;
    while (--count >= 0) {
        crc = crc ^ (int)*ptr++ << 8;
        for (i = 0; i < 8; ++i) {
            if (crc & 0x8000) {
                crc = crc << 1 ^ 0x1021;
            } else {
                crc = crc << 1;
            }
        }
    }
    return (CRC & 0xFFFF);
}
```

B.1.16 Error Injection

To enable validation of error handling on the Host, error injection support is required. Error injection support shall be available in non-production firmware images. The ONE_TIME_USE bit in INJECT_ERROR_TYPE (page 2 offset 0x68) determines whether the injected failure is for the next instance of the operation or for all subsequent instances of the operation until the error injection is disabled. The following error injection support shall be supported by the module.

- Force a catastrophic save and erase operation failure.
- Force an internal controller error.
- Force a permanent hardware failure.
- Force a NVM lifetime percentage value lower than the warning and error threshold.
- Inject a certain percentage of errors during writes to the NVM subsystem.
- Force an Energy Source failure if the module is using a local or tethered Energy Source.
- Force an Energy Source assessment failure if the module is using a local or tethered Energy Source.
- Force an Energy Source lifetime percentage value lower than the warning and error threshold if the module is using a local or tethered Energy Source.
- Force an Energy Source temperature higher than the warning and error threshold if the module is using a local or tethered Energy Source.
- Force a commit error during firmware update.
- Force a firmware image checksum error.
- Force an invalid firmware image error.

Error injection shall take place during the next instance of the applicable operation. Any enabled error injection shall be persisted across power cycles and resets until explicitly disabled by the Host or by the Factory Default operation. Error injection shall be disabled by default.

B.1.17 Statistics

Modules may provide statistics on the following operations.

- Duration of the last Catastrophic Save and Erase operations.
- Count of the completed Catastrophic Save and Erase operations over the module lifetime.
- Count of module power cycles over the module lifetime.

Additional statistics may be available in vendor specific registers.

B.1.18 Thermal

An SPD with thermal sensor that complies with TSE2004 Device Specification shall be required. Modules may have multiple thermal sensors monitoring temperature of various components on the module. Additional thermal sensors are supported through vendor specific registers.

Temperature measurement shall have a minimum resolution of 0.25 Celsius. Registers containing measured temperature value shall be 16-bits and report temperature as a 10-bit value based on the following definition.

Table 130 - Temperature value bit definition

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Reserved	Reserved	Reserved	Reserved	128	64	32	16
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8	4	2	1	0.5	0.25	Reserved	Reserved

Examples:

A temperature value of 10.5 Celsius is represented as 0000000010101000b.

A temperature value of 64.75 Celsius is represented as 0000010000001100b.

B.1.19 Host Area

Modules shall provide persistent storage to hosts to store data that applies to the module but can only be detected by a Host. Modules do not act upon any of these data.

B.1.20 Vendor Log Page

A module shall support a Vendor Log Page that provides information useful to triage issues seen on the module. A module may continue to use the `VENDOR_LOG_PAGE_SIZE` register in page 0 to communicate the number of valid vendor-specific bytes by specifying a non-zero value. If the module uses the `VENDOR_LOG_PAGE_SIZE` to communicate the number of valid bytes, the size is limited to a maximum value of 8160 bytes

To read the Vendor Log Page data, the Host should follow the **Reading Typed Block Data** workflow.

B.1.21 Vendor-Specific

A module may implement vendor-specific functionality beyond what is described in this specification. Vendor-specific functionalities are accessed through the vendor specific page(s) that may be supported by a module.

B.1.22 LCOM interface

A media controller indicates LCOM interface support by setting status Bit 7 LCOM Interface Supported in the `CAPABILITIES` register in page 0. If the optional LCOM interface is supported, the LCOM interface in `F0RC07` MCW register shall be compliant with DDR4RCD02 specification.

The host shall write the `LCOM_ENABLE` bit in `MODULE_OPS_CONFIG` register in page 0 as described in section NVDIMM Initialization Sequence in the DDR4RCD02 specification.

B.1.23 Label Data

A module shall support the Label Data Typed Block Data type. The Label Data Typed Block Data is a region on the module that is used by the Host to store metadata about how the memory exposed by the module is used. The Operation Unit size for the Label Data Typed Block Data type shall be 256 bytes.

A module shall support a minimum of 1024 bytes for the Label Data Typed Block Data type. For modules exposing more than 32GB of memory, the module shall support at least 256 bytes of additional data for every 32GB of memory usable by the Host. As an example, a module with 60GB of memory usable by the Host shall support at least 1280 bytes of Label Data Typed Block Data. A module with 150GB of memory usable by the Host shall support at least 2048 bytes of Label Data Typed Block Data.

B.2 Register Map

This section describes the I²C registers that are defined in each supported page.

The following conventions are used for registers defined in this specification.

- All register values are 0-based unless stated otherwise in the register description.
- All temperature register values are in Celsius.

B.2.1 Page 0 Register Map

The registers in page 0 are organized based on categories. Table 3 shows the layout of the categories in page 0.

Table 131 - Page 0 categories

Offset	Category	Description
0x00 – 0x03	Paging Mechanism	Registers related to I ² C page support.
0x04 – 0x0F	Version	Registers providing to version information.
0x10 – 0x3F	Characteristics	Registers providing characteristics information.
0x40 – 0x5F	Runtime Command	Registers related to runtime commands.
0x60 – 0x7F	Runtime Command Status	Registers providing runtime command status information.
0x80 – 0x87	Catastrophic Save	Registers providing Catastrophic Save information.
0x88 – 0x8F	Reserved	Reserved
0x90 – 0x9F	Thresholds	Registers related to thresholds.
0xA0 – 0xBF	Module	Registers providing module related information.
0xC0 – 0xEF	NVM Subsystem	Registers providing NVM subsystem related information.
0xF0 – 0xFF	Reserved	Reserved

Table 4 shows the registers that are in page 0.

Table 132 - Page 0 register map

Offset	Register Name	Host Access Property	Mandatory	Persistent Across Power Cycles
0x00	OPEN_PAGE	RW	Y	N
0x01	STD_NUM_PAGES	RO	Y	Y
0x02	VENDOR_START_PAGES	RO	Y	Y
0x03	VENDOR_NUM_PAGES	RO	Y	Y
0x04	HWREV	RO	Y	Y
0x05	Reserved			
0x06	SPECREV	RO	Y	Y
0x07	SLOT0_FWREV0	RO	Y	Y
0x08	SLOT0_FWREV1	RO	Y	Y
0x09	SLOT1_FWREV0	RO	Y	Y
0x0A	SLOT1_FWREV1	RO	Y	Y
0x0B-0x0F	Reserved			
0x10	CAPABILITIES	RO	Y	Y
0x11	CAPABILITIES1	RO	Y	Y

0x12-0x13	Reserved			
0x14	ENERGY_SOURCE_POLICY	RO	Y	Y
0x15	HOST_MAX_OPERATION_RETRY	RO	Y	Y
0x16	CSAVE_TRIGGER_SUPPORT	RO	Y	Y
0x17	EVENT_NOTIFICATION_SUPPORT	RO	Y	Y
0x18	Reserved	RO	Y	Y
0x19	Reserved	RO	Y	Y
0x1A	PAGE_SWITCH_LATENCY0	RO	Y	Y
0x1B	PAGE_SWITCH_LATENCY1	RO	Y	Y
0x1C	Reserved	RO	Y	Y
0x1D	Reserved	RO	Y	Y
0x1E	ERASE_TIMEOUT0	RO	Y	Y
0x1F	ERASE_TIMEOUT1	RO	Y	Y
0x20	Reserved	RO	Y	Y
0x21	Reserved	RO	Y	Y
0x22	FIRMWARE_OPS_TIMEOUT0	RO	Y	Y
0x23	FIRMWARE_OPS_TIMEOUT1	RO	Y	Y
0x24	ABORT_CMD_TIMEOUT	RO	Y	Y
0x25	MIN_OPERATING_TEMP	RO	Y	Y
0x26	MAX_OPERATING_TEMP	RO	Y	Y
0x27	MAX_RUNTIME_POWER0	RO	N	Y
0x28	MAX_RUNTIME_POWER1	RO	N	Y
0x29	Reserved	RO	N	Y
0x2A	Reserved	RO	N	Y
0x2B	CSAVE_IDLE_POWER_REQ0	RO	N	Y
0x2C	CSAVE_IDLE_POWER_REQ1	RO	N	Y
0x2D	CSAVE_MIN_VOLT_REQ0	RO	N	Y
0x2E	CSAVE_MIN_VOLT_REQ1	RO	N	Y
0x2F	CSAVE_MAX_VOLT_REQ0	RO	N	Y
0x30	CSAVE_MAX_VOLT_REQ1	RO	N	Y
0x31	VENDOR_LOG_PAGE_SIZE	RO	N	Y
0x32	REGION_BLOCK_SIZE	RO	Y	Y
0x33	OPERATIONAL_UNIT_OPS_TIMEOUT 0	RO	Y	Y
0x34	OPERATIONAL_UNIT_OPS_TIMEOUT 1	RO	Y	Y
0x35-0x3F	Reserved			
0x40	NVDIMM_MGT_CMD0	WO	Y	N
0x41	NVDIMM_MGT_CMD1	WO	Y	N
0x42	Reserved			
0x43	NVDIMM_FUNC_CMD0	WO	Y	N

0x44	Reserved			
0x45	Reserved	WO	Y	N
0x46	Reserved			
0x47	SET_EVENT_NOTIFICATION_CMD	WO	Y	N
0x48	Reserved			
0x49	SET_ES_POLICY_CMD	WO	N	N
0x4A	FIRMWARE_OPS_CMD	WO	Y	N
0x4B	OPERATIONAL_UNIT_OPS_CMD	WO	Y	N
0x4C-5F	Reserved			
0x60	NVDIMM_READY	RO	Y	N
0x61	NVDIMM_CMD_STATUS0	RO	Y	N
0x62	NVDIMM_CMD_STATUS1	RO	Y	N
0x63	Reserved			
0x64	SAVE_STATUS0	RO	Y	Y
0x65	Reserved			
0x66	Reserved	RO	Y	N
0x67	Reserved			
0x68	ERASE_STATUS0	RO	Y	N
0x69	Reserved			
0x6A	Reserved	RO	Y	N
0x6B	Reserved			
0x6C	FACTORY_DEFAULT_STATUS0	RO	Y	N
0x6D	Reserved			
0x6E	SET_EVENT_NOTIFICATION_STATU S0	RO	Y	N
0x6F	Reserved			
0x70	SET_ES_POLICY_STATUS	RO	Y	N
0x71	FIRMWARE_OPS_STATUS	RO	Y	N
0x72	OPERATIONAL_UNIT_OPS_STATUS	RO	Y	N
0x73-0x7F	Reserved			
0x80	CSAVE_INFO0	RO	Y	Y
0x81-0x83	Reserved			
0x84	CSAVE_FAIL_INFO0	RO	Y	Y
0x85	CSAVE_FAIL_INFO1	RO	Y	Y
0x86 – 0x8 F	Reserved			
0x90	NVM_LIFETIME_ERROR_THRESHOL D	RO	Y	Y
0x91	ES_LIFETIME_ERROR_THRESHOLD	RO	N	Y
0x92	ES_TEMP_ERROR_THRESHOLD	RO	N	Y
0x93 - 0x97	Reserved			
0x98	NVM_LIFETIME_WARNING_THRESH OLD	RW	Y	Y

0x99	ES_LIFETIME_WARNING_THRESHOLD	RW	N	Y
0x9A	ES_TEMP_WARNING_THRESHOLD	RW	N	Y
0x9B-0x9F	Reserved			
0xA0	MODULE_HEALTH	RO	Y	N
0xA1	MODULE_HEALTH_STATUS0	RO	Y	N
0xA2	MODULE_HEALTH_STATUS1	RO	Y	N
0xA3-0xA4	Reserved			
0xA5	ERROR_THRESHOLD_STATUS	RO	Y	N
0xA6	Reserved			
0xA7	WARNING_THRESHOLD_STATUS	RO	Y	N
0xA8	Reserved			
0xA9	AUTO_ES_HEALTH_FREQUENCY	RW	N	Y
0xAA	MODULE_OPS_CONFIG	RW	Y	N
0xAB-0xBF	Reserved			
0xC0	NVM_LIFETIME	RO	Y	Y
0xC1-0xC7	Reserved			
0xC8-0xC9	WRITE_DATA_POLICY	RW	Y	N
0xE0-0xEF	CSAVE_POWER_REQ_x	RO	Y	Y
0xF0-0xFF	CSAVE_TIMEOUT_x	RO	Y	Y

B.2.1.1 Paging Mechanism Registers

The registers in this section are related to the I²C paging mechanism supported by the module.

A) OPEN_PAGE – Offset 0x00

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Open page number	RW	Y	N	0

When the OPEN_PAGE register is read, it returns the current opened page number. When the OPEN_PAGE register is written to, the module shall attempt to set the current opened page number to the value written. The default value of OPEN_PAGE shall be 0.

B) STD_NUM_PAGES – Offset 0x01

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of standard pages supported	RO	Y	Y	4

The STD_NUM_PAGES register returns the number of standard defined pages supported by the module. This register shall return the value 4.

C) **VENDOR_START_PAGES** – Offset 0x02

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Start page number for vendor-specific pages supported	RO	Y	Y	>= 4

The **VENDOR_START_PAGES** register returns the starting page number for vendor-specific pages. The value returned from this register shall be greater than or equal to the value returned from **STD_NUM_PAGES** register. If the module does not support any vendor-specific pages, the value returned from this register shall be equal to the value returned from **STD_NUM_PAGES** register.

D) **VENDOR_NUM_PAGES** – Offset 0x03

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of vendor-specific pages supported	RO	Y	Y	Implementation-specific

The **VENDOR_NUM_PAGES** register returns the number of vendor-specific pages supported by the module. If an implementation does not support any vendor-specific pages, the value returned shall be 0.

B.2.1.2 Version Registers

The registers in this section provide version information about the module.

1) **HWREV** – Offset 0x04

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Controller hardware revision	RO	Y	Y	Implementation-specific

The **HWREV** register returns the controller hardware revision.

2) **SPECREV** – Offset 0x06

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[3:0] Minor Revision [7:4] Major Revision	RO	Y	Y	Implementation-specific

The **SPECREV** register returns the specification version supported by the module. Both the major and minor version of the specification supported shall be provided.

Examples

If the module implements specification version 1.0, the value returned from this register shall be 00010000b.

If the module implements specification version 2.0, the value returned from this register shall be 00020000b.

3) SLOT0_FWREV0 – Offset 0x07

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Slot 0 controller firmware revision LSB	RO	Y	Y	Implementation-specific

The SLOT0_FWREV0 register returns the least significant byte of the controller firmware revision of the firmware image in slot 0. The SLOT0_FWREV0 register is not impacted by the Factory Default operation.

The combination of the values returned by SLOT0_FWREV0 and SLOT0_FWREV1 shall be non-zero. Controller firmware revision value shall be assigned in increasing order so that a larger revision value represents a more recent firmware image.

4) SLOT0_FWREV1 – Offset 0x08

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Slot 0 controller firmware revision MSB	RO	Y	Y	Implementation-specific

The SLOT0_FWREV1 register returns the most significant byte of the controller firmware revision of the firmware image in slot 0. The SLOT0_FWREV1 register is not impacted by the Factory Default operation.

The combination of the values returned by SLOT0_FWREV0 and SLOT0_FWREV1 shall be non-zero. Controller firmware revision value shall be assigned in increasing order so that a larger revision value represents a more recent firmware image.

5) SLOT1_FWREV0 – Offset 0x09

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Slot 1 controller firmware revision LSB	RO	Y	Y	0

The SLOT1_FWREV0 register returns the least significant byte of the controller firmware revision of the firmware image in slot 1. If slot 1 does not contain a firmware image or contains an invalid firmware image, the value returned shall be 0. The SLOT1_FWREV0 register is not impacted by the Factory Default operation.

6) SLOT1_FWREV1 – Offset 0x0A

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Slot 1 controller firmware revision MSB	RO	Y	Y	0

The SLOT1_FWREV1 register returns the most significant byte of the controller firmware revision of the firmware image in slot 1. If slot 1 does not contain a firmware image or contains an invalid firmware image, the value returned shall be 0. The SLOT1_FWREV1 register is not impacted by the Factory Default operation.

B.2.1.3 Characteristics Registers

The registers in this section provide characteristics information supported by the module.

1) CAPABILITIES – Offset 0x10

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Event Notification Supported [1] : Auto Energy Source Health Check Supported [2] : Error Injection Supported [3] : Device Statistics Supported [4] : I ² C Block Command Supported [5]: Two-pulse SAVE_N Trigger Mode Supported [6]: Three-pulse SAVE_N Trigger Mode Supported [7] LCOM Interface Supported	RO	Y	Y	Implementation-specific

The CAPABILITIES register provides information regarding the capabilities supported by the module. A bit set to 1 indicates that the module supports the corresponding capability. A bit set to 0 indicates the module does not support the corresponding capability.

If Bit 0, Event Notification Supported, is set, module supports asserting the EVENT_N pin when an enabled event occurs.

If Bit 1, Auto Energy Source Health Check, is set, module will do periodic Energy Source health check.

If Bit 2, Error Injection Supported, is set, module supports error injection.

If Bit 3, Device Statistics Supported, is set, module supports collecting the device statistics defined in this specification.

If Bit 4, I²C Block Command Supported, is set, module supports the I²C Block Read and I²C Block Write operation.

If Bit 5, Two-pulse SAVE_N Trigger Mode Supported, is set, the module supports two-pulse SAVE_N trigger mode. For a detailed description of this feature see MODULE_OPS_CONFIG – Offset 0xAA.

If Bit 6, Three-pulse SAVE_N Trigger Mode Supported, is set, the module supports three-pulse SAVE_N trigger mode. For a detailed description of this feature see MODULE_OPS_CONFIG – Offset 0xAA.

If Bit 7, LCOM Interface Supported, is set, the module supports the LCOM interface.

2) CAPABILITIES1 – Offset 0x11

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Reserved [1] : Abort CMD Timeout in Seconds [2] : Operational Unit Buffer Per Typed Block Data [7:3] : Reserved	RO	Y	Y	Implementation-specific

If Bit 0, Reserved.

If Bit 1, Abort CMD Timeout in Seconds, is set, the abort timeout value listed in the ABORT_CMD_TIMEOUT register is in units of seconds. If Bit 1 is cleared, the abort timeout value listed in the ABORT_CMD_TIMEOUT register is in units of milliseconds.

If Bit 2, Operational Unit Buffer Per Typed Block Data, is set, the module supports an Operational Unit buffer for each Typed Block Data type.

3) ENERGY_SOURCE_POLICY – Offset 0x14

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Device Managed Policy supported [1] : Host Managed Policy supported [7:2] : Reserved	RO	Y	Y	Non-zero value

The ENERGY_SOURCE_POLICY register provides information regarding the Energy Source policy supported by the module. A bit set to 1 indicates that the module supports the corresponding policy. A bit set to 0 indicates the module does not support the corresponding policy.

In Device Managed Policy, the module is responsible for the management of the Energy Source used for the Catastrophic Save operation. In Host Managed Policy, the Host is responsible for the management of the Energy Source used for the Catastrophic Save operation.

The default value shall be a non-zero value as either Device Managed Policy or Host Managed Policy shall be supported. A module may support both policies.

4) HOST_MAX_OPERATION_RETRY – Offset 0x15

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[1:0] : Maximum Catastrophic Save retry count [3:2] : Reserved [5:4] : Maximum Erase retry count [7:6] : Reserved	RO	Y	Y	Non-zero

The HOST_MAX_OPERATION_RETRY register provides the recommended retry count to the Host if a Catastrophic Save, Erase operation fails or exceeds the maximum timeout value.

After the Host issue the Erase operation, the Host shall wait for the max erase time specified in the ERASE_TIMEOUT0 and ERASE_TIMEOUT1 registers before issuing a subsequent Erase operation.

5) CSAVE_TRIGGER_SUPPORT – Offset 0x16

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : SAVE_N [7:1] : Reserved	RO	Y	Y	Non-zero

The CSAVE_TRIGGER_SUPPORT register provides the Catastrophic Save triggers supported by the module. A bit set to 1 indicates that the module supports the corresponding trigger. A bit set to 0 indicates the module does not support the corresponding trigger.

If the SAVE_N trigger is supported, the module shall trigger the Catastrophic Save operation based on the SAVE_N pin behavior defined in 8.1.8.7.

The default value shall be a non-zero value as the SAVE_N trigger shall be supported. A module may support more than one trigger.

6) EVENT_NOTIFICATION_SUPPORT – Offset 0x17

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Persistency notification [1] : Warning threshold notification [2] : Voltage regulator failed notification [7:3] : Reserved	RO	Y	Y	0 (event notification not supported) 1,3,5 or 7 (event notification supported)

The EVENT_NOTIFICATION_SUPPORT register provides information on the events that the module will generate notification for. A bit set to 1 indicates that the module supports generating a notification if the corresponding event occurs. A bit set to 0 indicates the module does not support generating a notification if the corresponding event occurs.

If the Persistency notification is supported, module shall generate a notification if there is a persistency loss or restored event.

If the Warning threshold notification is supported, module shall generate a notification if there is a threshold exceeded or below threshold event.

If the Voltage regulator failed notification is supported, module shall generate a notification if voltage regulator on the module fails.

7) PAGE_SWITCH_LATENCY0 – Offset 0x1A

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Host wait time for I ² C page switch completion latency LSB	RO	Y	Y	Implementation-specific

The PAGE_SWITCH_LATENCY0 register provides the least significant byte of the Host wait time for the I²C page switch completion latency. Host shall use the PAGE_SWITCH_LATENCY0 and PAGE_SWITCH_LATENCY1 register values when executing an I²C page switch operation.

8) PAGE_SWITCH_LATENCY1 – Offset 0x1B

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
<p>[6:0] : Host wait time for I²C page switch completion latency MSB</p> <p>[7] : 0 – Indicates completion latency value is in units of milliseconds.</p> <p>1 – Indicates completion latency value is in units of seconds.</p>	RO	Y	Y	Implementation-specific

The PAGE_SWITCH_LATENCY1 register provides the most significant byte of the Host wait time for the I²C page switch completion latency. Host shall use the PAGE_SWITCH_LATENCY0 and PAGE_SWITCH_LATENCY1 register values when executing an I²C page switch operation.

If Bit 7 is 0, the completion latency value is in units of milliseconds. If Bit 7 is 1, the completion latency value is in units of seconds.

9) ERASE_TIMEOUT0 – Offset 0x1E

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
<p>[7:0] : Worst case Erase completion latency LSB</p>	RO	Y	Y	Implementation-specific

The ERASE_TIMEOUT0 register provides the least significant byte of the worst case Erase completion latency in milliseconds or seconds. Host should use the ERASE_TIMEOUT0 and ERASE_TIMEOUT1 registers to determine when an Erase operation has timed out.

10) ERASE_TIMEOUT1 – Offset 0x1F

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
<p>[6:0] : Worst case Erase completion latency MSB</p> <p>[7] : 0 – Indicates completion latency value is in units of milliseconds.</p> <p>1 – Indicates completion latency value is in units of seconds.</p>	RO	Y	Y	Implementation-specific

The ERASE_TIMEOUT1 register provides the most significant byte of the worst case Erase completion latency and the time unit for the worst case completion latency. Host should use the ERASE_TIMEOUT0 and ERASE_TIMEOUT1 registers to determine when an Erase operation has timed out.

If Bit 7 is 0, the worst case completion latency value is in units of milliseconds. If Bit 7 is 1, the worst case completion latency value is in units of seconds.

11) FIRMWARE_OPS_TIMEOUT0 – Offset 0x22

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Worst case Firmware Operations completion latency LSB	RO	Y	Y	Implementation-specific

The FIRMWARE_OPS_TIMEOUT0 register provides the least significant byte of the worst case Firmware Operations completion latency in milliseconds or seconds. Host should use the FIRMWARE_OPS_TIMEOUT0 and FIRMWARE_OPS_TIMEOUT1 registers to determine when a Firmware Operations operation has timed out.

12) FIRMWARE_OPS_TIMEOUT1 – Offset 0x23

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[6:0] : Worst case Firmware Operations completion latency MSB [7] : 0 – Indicates completion latency value is in units of milliseconds. 1 – Indicates completion latency value is in units of seconds.	RO	Y	Y	Implementation-specific

The FIRMWARE_OPS_TIMEOUT1 register provides the most significant byte of the worst case Firmware Operations completion latency and the time unit for the worst case completion latency. Host should use the FIRMWARE_OPS_TIMEOUT0 and FIRMWARE_OPS_TIMEOUT1 registers to determine when a Firmware Operations operation has timed out.

If Bit 7 is 0, the worst case completion latency value is in units of milliseconds. If Bit 7 is 1, the worst case completion latency value is in units of seconds.

13) ABORT_CMD_TIMEOUT – Offset 0x24

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Maximum time to abort a running command	RO	Y	Y	Implementation-specific

The ABORT_CMD_TIMEOUT register provides the maximum time in milliseconds to abort a running command. Host should use the ABORT_CMD_TIMEOUT register to determine when an abort operation has timed out. The resolution of this register can be determined by reading Bit 1, Abort CMD Timeout in Seconds, in the CAPABILITIES1(0x11) register. If this bit is set, the units are in seconds, and if it is cleared, the units are in milliseconds.

14) MIN_OPERATING_TEMP – Offset 0x25

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Minimum operating temperature in Celsius.	RO	Y	Y	Implementation-specific

The MIN_OPERATING_TEMP register provides the minimum operating temperature in Celsius.

15) MAX_OPERATING_TEMP – Offset 0x26

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Maximum operating temperature in Celsius.	RO	Y	Y	Implementation-specific

The MAX_OPERATING_TEMP register provides the maximum operating temperature in Celsius.

16) MAX_RUNTIME_POWER0 – Offset 0x27

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Maximum runtime power consumption from the 12V pin in milliwatts LSB.	RO	N	Y	Implementation-specific

The MAX_RUNTIME_POWER0 register provides the least significant byte of the maximum runtime power consumption from the 12V pin in milliwatts. A module may draw power from the 12V pin to charge an Energy Source connected to the module or to provide power to components on the module.

This register shall be supported if the module supports Host Managed Policy or if module draws power from the 12V pin to charge an Energy Source connected to the module.

17) MAX_RUNTIME_POWER1 – Offset 0x28

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Maximum runtime power consumption from the 12V pin in milliwatts MSB.	RO	N	Y	Implementation-specific

The MAX_RUNTIME_POWER1 register provides the most significant byte of the maximum runtime power consumption from the 12V pin in milliwatts. A module may draw power from the 12V pin to charge an Energy Source connected to the module or to provide power to components on the module.

This register shall be supported if the module supports Host Managed Policy or if module draws power from the 12V pin to charge an Energy Source connected to the module.

18) CSAVE_IDLE_POWER_REQ0 – Offset 0x2B

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Average power required after the Catastrophic Save operation completes in milliwatts LSB.	RO	N	Y	Implementation-specific

The CSAVE_IDLE_POWER_REQ0 register provides the least significant byte of the average power required by the module after the Catastrophic Save operation completes in milliwatts.

For a Host that uses shared Energy Source, Host should use the CSAVE_IDLE_POWER_REQ0 and CSAVE_IDLE_POWER_REQ1 register values for energy budgeting.

This register shall be supported if the module supports Host Managed Policy.

19) CSAVE_IDLE_POWER_REQ1 – Offset 0x2C

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Average power required after the Catastrophic Save operation completes in milliwatts MSB.	RO	N	Y	Implementation-specific

The CSAVE_IDLE_POWER_REQ1 register provides the most significant byte of the average power required by the module after the Catastrophic Save operation completes in milliwatts.

For a Host that use shared Energy Source, Host should use the CSAVE_IDLE_POWER_REQ0 and CSAVE_IDLE_POWER_REQ1 register values for energy budgeting.

This register shall be supported if the module supports Host Managed Policy.

20) CSAVE_MIN_VOLT_REQ0 – Offset 0x2D

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Minimum voltage the Energy Source has to service during a Catastrophic Save operation in millivolt LSB.	RO	N	Y	Implementation-specific

The CSAVE_MIN_VOLT_REQ0 register provides the least significant byte of the minimum voltage in millivolts the Energy Source has to service during a Catastrophic Save operation.

This register shall be supported if the module supports Host Managed Policy. Modules shall support a value of 16A8h (5800) or smaller for the CSAVE_MIN_VOLT_REQ0 and CSAVE_MIN_VOLT_REQ1 registers.

21) CSAVE_MIN_VOLT_REQ1 – Offset 0x2E

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Minimum voltage the Energy Source has to service during a Catastrophic Save operation millivolt MSB.	RO	N	Y	Implementation-specific

The CSAVE_MIN_VOLT_REQ1 register provides the most significant byte of the minimum voltage in millivolts the Energy Source has to service during a Catastrophic Save operation.

This register shall be supported if the module supports Host Managed Policy. Modules shall support a value of 16A8h (5800) or smaller for the CSAVE_MIN_VOLT_REQ0 and CSAVE_MIN_VOLT_REQ1 registers.

22) CSAVE_MAX_VOLT_REQ0 – Offset 0x2F

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Maximum voltage the Energy Source has to service during a Catastrophic Save operation in millivolt LSB.	RO	N	Y	Implementation-specific

The CSAVE_MAX_VOLT_REQ0 register provides the least significant byte of the maximum voltage in millivolts the Energy Source has to service during a Catastrophic Save operation.

This register shall be supported if the module supports Host Managed Policy. Modules shall support a value of 35E8h (13800) or smaller for the CSAVE_MAX_VOLT_REQ0 and CSAVE_MAX_VOLT_REQ1 registers.

23) CSAVE_MAX_VOLT_REQ1 – Offset 0x30

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Maximum voltage the Energy Source has to service during a Catastrophic Save operation millivolt MSB.	RO	N	Y	Implementation-specific

The CSAVE_MAX_VOLT_REQ1 register provides the most significant byte of the maximum voltage in millivolts the Energy Source has to service during a Catastrophic Save operation.

This register shall be supported if the module supports Host Managed Policy. Modules shall support a value of 35E8h (13800) or smaller for the CSAVE_MAX_VOLT_REQ0 and CSAVE_MAX_VOLT_REQ1 registers.

24) VENDOR_LOG_PAGE_SIZE – Offset 0x31

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Vendor Log Page size in 32 bytes multiple.	RO	N	Y	Implementation-specific

The VENDOR_LOG_PAGE_SIZE register provides the size in 32 bytes multiple of the Vendor Log Page. The Vendor Log Page provides implementation specific diagnostic data that may be helpful to root cause issues on the module. If the module does not support a Vendor Log Page, this register shall return a data payload of all 0.

25) REGION_BLOCK_SIZE – Offset 0x32

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Region size in 32 bytes multiple.	RO	Y	Y	>= 8

The REGION_BLOCK_SIZE register provides the supported region size in 32 bytes multiple. Region is used in I²C block operations to transfer data between the Host and the module. The minimum value supported shall be 8. The maximum region size is 8160 bytes.

Example: A REGION_BLOCK_SIZE register value of 32 indicates that the module's region block size is 1024 bytes (i.e., 32 * 32).

26) OPERATIONAL_UNIT_OPS_TIMEOUT0 – Offset 0x33

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Worst case Operational Unit Operations completion latency LSB	RO	Y	Y	Implementation-specific

The OPERATIONAL_UNIT_OPS_TIMEOUT0 register provides the least significant byte of the worst case Operational Unit Operations completion latency in milliseconds or seconds. The Host should use the OPERATIONAL_UNIT_OPS_TIMEOUT0 and OPERATIONAL_UNIT_OPS_TIMEOUT1 registers to determine when an Operational Unit Operations operation has timed out.

27) OPERATIONAL_UNIT_OPS_TIMEOUT1 – Offset 0x34

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[6:0] : Worst case Operational Unit Operations completion latency MSB [7] : 0 – Indicates completion latency value is in units of milliseconds. 1 – Indicates completion latency value is in units of seconds.	RO	Y	Y	Implementation-specific

The OPERATIONAL_UNIT_OPS_TIMEOUT0 register provides the most significant byte of the worst case Operational Unit Operations completion latency in milliseconds or seconds. The Host should use the OPERATIONAL_UNIT_OPS_TIMEOUT0 and OPERATIONAL_UNIT_OPS_TIMEOUT1 registers to determine when an Operational Unit Operations operation has timed out.

If Bit 7 is 0, the worst case completion latency value is in units of milliseconds. If Bit 7 is 1, the worst case completion latency value is in units of seconds.

B.2.1.4 Runtime Command Registers

The registers in this section are related to runtime commands supported by the module.

1) NVDIMM_MGT_CMD0 – Offset 0x40

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : RST_CTRL - Reset Controller [1] : CL_ALL_CMD_STAT - Clear all Command Status registers [2] : CL_SAVE_STAT - Clear save status register [3] : Reserved [4] : CL_ERASE_STAT - Clear erase status register [5] : Reserved [6] : CL_SET_EVENT_NOTIFICATION_STAT - Clear set event notification status register [7] : CL_SET_ES_STAT - Clear set Energy Source status register	WO	Y	N	N/A

The NVDIMM_MGT_CMD0 register allows a Host to reset the controller or clear command status register(s) on the module. To initiate an operation, Host shall set the bit corresponding to the operation desired and issue an I²C write byte operation to this register. If the RST_CTRL or CL_ALL_CMD_STAT bit is set, the module shall ignore all other bits in this register. If both RST_CTRL and CL_ALL_CMD_STAT bits are set, module shall ignore the CL_ALL_CMD_STAT bit. The NV Controller self clears the bit(s) after it executes the command.

If Bit 0, RST_CTRL, is set, module shall initiate a reset on the controller.

If Bit 1, CL_ALL_CMD_STAT, is set, module shall

- Clear all in progress bits in NVDIMM_CMD_STATUS0 register (offset 0x61 in page 0).
- Set SAVE_STATUS0 register (offset 0x64 in page 0) to 0.
- Set ERASE_STATUS0 register (offset 0x68 in page 0) to 0.
- Set FACTORY_DEFAULT_STATUS0 register (offset 0x6C in page 0) to 0.
- Clear Bits 0 and 1 in SET_EVENT_NOTIFICATION_STATUS0 register (offset 0x6E in page 0).
- Clear Bits 0 and 1 in SET_ES_POLICY_STATUS register (offset 0x70 in page 0).
- Clear all bits except Bit 2 in FIRMWARE_OPS_STATUS register (offset 0x71 in page 0).

If Bit 2, CL_SAVE_STAT, is set, module shall set SAVE_STATUS0 register (offset 0x64 in page 0) to 0.

If Bit 3, Reserved

If Bit 4, CL_ERASE_STAT, is set, module shall set ERASE_STATUS0 register (offset 0x68 in page 0) to 0.

If Bit 5, Reserved.

If Bit 6, CL_SET_EVENT_NOTIFICATION_STAT, is set, module shall clear Bits 0 and 1 in SET_EVENT_NOTIFICATION_STATUS0 register (offset 0x6E in page 0).

If Bit 7, CL_SET_ES_STAT, is set, module shall clear Bits 0 and 1 in SET_ES_POLICY_STATUS register (offset 0x70 in page 0).

2) NVDIMM_MGT_CMD1 – Offset 0x41

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : CL_FACTORY_DEFAULT_STAT - Clear Factory Default status register	WO	Y	N	N/A
[1] : CL_FIRMWARE_OPS_STAT - Clear Firmware Ops status register				
[2] : DEASSERT_EVENT – Do not assert the EVENT_N pin				
[3] : CL_OPERATIONAL_UNIT_OPS_STAT – Clear Operational Unit Ops status register				
[7:4] : Reserved				

The NVDIMM_MGT_CMD1 register allows a Host to clear command status register(s) on the module. To initiate an operation, Host shall set the bit corresponding to the operation desired and issue an I²C write byte operation to this register. The NV Controller self clears the bit(s) after it executes the command.

If Bit 0, CL_FACTORY_DEFAULT_STAT, is set, module shall set FACTORY_DEFAULT_STATUS0 register (offset 0x6C in page 0) to 0.

If Bit 1, CL_FIRMWARE_OPS_STAT, is set, module shall clear all bits except Bit 2 in FIRMWARE_OPS_STATUS register (offset 0x71 in page 0).

If Bit 2, DEASSERT_EVENT, is set, module shall not assert the EVENT_N pin.

If Bit 3, CL_OPERATIONAL_UNIT_OPS_STAT, is set, module shall set OPERATIONAL_UNIT_OPS_STATUS register (offset 0x72 in page 0) to 0.

3) NVDIMM_FUNC_CMD0 – Offset 0x43

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : START_FACTORY_DEFAULT: Start a Factory Default Operation [1] : START_SAVE : Start a Catastrophic Save Operation [2] : Reserved [3] : START_ERASE : Start an Erase Operation [4] : ABORT_CURRENT_OP : Abort the Current Operation, if any [7:5] : Reserved	WO	Y	N	N/A

The NVDIMM_FUNC_CMD0 register allows a Host to initiate a Factory Default, Catastrophic Save, Erase or Abort operation on the module. To initiate an operation, Host shall set the bit corresponding to the operation desired and issue an I²C write byte operation to this register. Upon receipt of the I²C write byte operation, the module shall update the corresponding in progress bit in the NVDIMM_CMD_STATUS0 register (offset 0x61 in page 0). When the operation completes, the module shall clear the corresponding in progress bit in NVDIMM_CMD_STATUS0 register and update the corresponding command status register, if any. Only one bit can be set at any one time. If more than one bit is set, the module shall ignore the request. The NV Controller self clears the bit(s) after it executes the command.

If Bit 0, START_FACTORY_DEFAULT, is set, the module shall start the Factory Default operation.

If Bit 1, START_SAVE, is set, the module shall start the Catastrophic Save operation. On the start of the Catastrophic Save operation, module shall set Bit 1, START_SAVE_CMD, to 1 and set Bits 2 to 0 in the CSAVE_INFO0 register (offset 0x80 in page 0).

If Bit 2, Reserved.

If Bit 3, START_ERASE, is set, the module shall start the Erase operation. Upon the start of an Erase operation, the module shall set Bit 0, NVM_Data_Valid, in the CSAVE_INFO0 register (offset 0x80 in page 0) to 0.

If Bit 4, ABORT_CURRENT_OP, is set, the module shall abort the current operation that is in progress.

4) SET_EVENT_NOTIFICATION_CMD – Offset 0x47

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Persistency notification [1] : Warning threshold notification [2] : Voltage regulator failed notification [7:2] : Reserved	WO	Y	N	N/A

The SET_EVENT_NOTIFICATION_CMD register allows a Host to enable or disable notification for the specified event(s). To enable event notification, Host shall set the bit(s) corresponding to the event(s) desired. To disable event notification, Host shall clear the bit(s) corresponding to the event(s) desired. When the operation completes, module shall update the SET_EVENT_NOTIFICATION_STATUS0 register (offset 0x6E in page 0).

If Bit 0, Persistency notification, is set, module shall generate a notification by driving EVENT_N pin low if the module detects a lost persistency or persistency restored event. See MODULE_HEALTH – Offset 0xA0 for information on when these events occur.

If Bit 1, Warning threshold notification, is set, module shall generate a notification by driving EVENT_N pin low if a warning threshold exceeded or below warning threshold event occurs. See MODULE_HEALTH – Offset 0xA0 for information on when these events occur.

If Bit 2, Voltage regulator failed notification, is set, module shall generate a notification by driving EVENT_N pin low if voltage regulator on the module fails.

If an event notification is disabled, module shall not generate a notification when the corresponding event occurred.

5) SET_ES_POLICY_CMD – Offset 0x49

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Device Managed Policy [1] : Host Managed Policy [7:2] : Reserved	WO	N	N	N/A

The SET_ES_POLICY_CMD register allows a Host to set the Energy Source policy on the module. Only a single bit can be set. To set the Energy Source policy, Host shall set the bit corresponding to the desired Energy Source policy. When the operation completes, module shall update the SET_ES_POLICY_STATUS register (offset 0x70 in page 0).

If Bit 0, Device Managed Policy, is set, module shall manage the Energy Source used for the Catastrophic Save operation.

If Bit 1, Host Managed Policy, is set, the Host shall manage the Energy Source used for the Catastrophic Save operation.

6) FIRMWARE_OPS_CMD – Offset 0x4A

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Firmware Update Mode - 0: Disable firmware update mode - 1: Enable firmware update mode [1] : Clear firmware data region [2] : Generate firmware data region checksum [3] : Commit firmware data region [4] : Validate firmware header [5] : Validate firmware image [7:6] : Reserved	WO	Y	N	N/A

The FIRMWARE_OPS_CMD register allows a Host to initiate firmware operations related commands. Only a single bit can be set. To initiate the desired operation, Host shall set the bit corresponding to the desired operation. On receipt of the I²C write byte operation, module shall update the FIRMWARE_OPS in progress bit in NVDIMM_CMD_STATUS0 register (offset 0x61 in page 0). When the operation completes, module shall clear the FIRMWARE_OPS in progress bit in NVDIMM_CMD_STATUS0 register and update the FIRMWARE_OPS_STATUS register (offset 0x71 in page 0).

Bit 0, Firmware Update Mode, allows the Host to enable or disable firmware update mode on the module. A set bit indicates a desire to enable firmware update mode. A clear bit indicates a desire to disable firmware update mode.

If Bit 1, Clear firmware image data region, is set, module shall set the firmware image data region to 0.

If Bit 2, Generate firmware image data region checksum, is set, module shall calculate the checksum of the contents of the firmware image data region and return the checksum value in FW_REGION_CRC0 (offset 0x40 in page 3) and FW_REGION_CRC1 (offset 0x41 in page 3) registers. The checksum shall be calculated using the algorithm described in Section B.1.15.1.

If Bit 3, Commit firmware image data region, is set, module shall commit the data in the firmware image data region to the corresponding location in the module where the firmware for slot 1 is located at.

If Bit 4, Validate firmware header, is set, module shall validate that common firmware header is applicable to the module.

If Bit 5, Validate firmware image, is set, module shall validate the size and calculated checksum of the firmware image in slot1 matches the size and checksum in the common firmware image header. The module may do additional checks to verify the firmware image in slot1 is valid. If the firmware image in slot1 is validated, module shall update SLOT1_FWREV0 and SLOT1_FWREV1 registers with the revision of the firmware image in slot1.

7) OPERATIONAL_UNIT_OPS_CMD – Offset 0x4B

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Get Operational Unit [1] : Set Operational Unit [2] : Clear Operational Unit Buffer [3] : Generate Operational Unit Checksum [7:4] : Reserved	WO	Y	N	N/A

The OPERATIONAL_UNIT_OPS_CMD register allows a Host to initiate Operational Unit operations related commands against a specific Typed Block Data. Only one bit can be set at any one time. To initiate the desired operation, the Host shall set the bit corresponding to the desired operation. Upon receipt of the I²C write byte operation, the module shall update the OPERATIONAL_UNIT_OPS in progress bit in NVDIMM_CMD_STATUS1 register (offset 0x62 in page 0). When the operation completes, the module shall clear the OPERATIONAL_UNIT_OPS in progress bit in NVDIMM_CMD_STATUS1 register and update the OPERATIONAL_UNIT_OPS_STATUS register (offset 0x72 in page 0).

If Bit 0, Get Operational Unit, is set, the module shall retrieve the Operational Unit identified by Operational Unit Id registers (offset 0xC and 0xD in page 3) for the Typed Block Data specified in the TYPED_BLOCK_DATA register (offset 0x4 in page 3) into an internal buffer.

If Bit 1, Set Operational Unit, is set, the module shall commit the data for the Operational Unit identified by Operational Unit Id registers (offset 0xC and 0xD in page 3) for the Typed Block Data specified in the TYPED_BLOCK_DATA register (offset 0x4 in page 3) to the corresponding location in the module.

If Bit 2, Clear Operational Unit Buffer, is set, the module shall set the internal buffer used for the Operational Unit corresponding to the Typed Block Data specified in the TYPED_BLOCK_DATA register (offset 0x4 in page 3) to all zeroes.

If Bit 3, Generate Operational Unit Checksum, is set, the module shall calculate the checksum of the contents of the internal buffer associated with the Operational Unit identified by Operational Unit Id registers (offset 0xC and 0xD in page 3) for the Typed Block Data specified in the TYPED_BLOCK_DATA register (offset 0x4 in page 3) and return the checksum value in OPERATIONAL_UNIT_CRC0 (offset 0x14 in page 3) and OPERATIONAL_UNIT_CRC1 (offset 0x15 in page 3) registers. The checksum shall be calculated using the algorithm described in Section B.1.15.1.

B.2.1.5 Runtime Command Status Registers

The registers in this section provide status information about runtime commands.

1) NVDIMM_READY – Offset 0x60

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Status value for NVDIMM controller	RO	Y	N	0

The NVDIMM_READY register provides information on whether the controller is ready for Host access after a reset. When the controller is ready for Host access, a value of 0xA5 shall be return. The meaning of all other values are implementation-specific. The NVDIMM_READY register is not impacted by the Factory Default operation.

After a power cycle or controller reset, the Host shall read this register and wait for the value of this register to be 0xA5 before accessing registers on the module. If the value of this register is not 0xA5, Host should only access offsets 0x0, 0x60, 0xA0 or 0xA1 in page 0 and shall not access registers in page 1, 2 or 3.

2) NVDIMM_CMD_STATUS0 – Offset 0x61

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : 0 - Controller NOT busy 1 – Controller busy with previous command. [1] : FACTORY_DEFAULT in Progress [2] : SAVE in Progress [3] : Reserved [4] : ERASE in Progress [5] : ABORT in Progress [6] : Reserved [7] : FIRMWARE_OPS in Progress	RO	Y	N	0

The NVDIMM_CMD_STATUS0 register provides information on the busy status of the controller and whether there are operations in progress.

If Bit 0 is set to 0, the controller is not executing any operations. If Bit 0 is set to 1, controller is busy executing an operation.

If Bit 1 is set to 1, the Factory Default operation is currently in progress.

If Bit 2 is set to 1, the Catastrophic Save operation is currently in progress.

If Bit 3 is reserved.

If Bit 4 is set to 1, the Erase operation is currently in progress.

If Bit 5 is set to 1, the Abort operation is currently in progress.

If Bit 6 is reserved.

If Bit 7 is set to 1, one of the Firmware Operations operation is currently in progress.

The module shall auto clear the in progress bits when the corresponding operation completes or when the Host requests to clear all status registers.

3) NVDIMM_CMD_STATUS1 – Offset 0x62

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : OPERATIONAL_UNIT_OPS in Progress [7:1] : Reserved	RO	Y	N	0

The NVDIMM_CMD_STATUS1 register provides information on whether there are operations in progress.

If Bit 0 is set to 1, one of the Operational Unit Operations operation is currently in progress.

The module shall auto clear the in progress bits when the corresponding operation completes or when the Host requests to clear all status registers.

4) SAVE_STATUS0 – Offset 0x64

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : SAVE_SUCCESS [1] : SAVE_ERROR [3:2] : Reserved [4] : ABORT_SUCCESS [5] : ABORT_ERROR [7:6] : Reserved	RO	Y	Y	0

The SAVE_STATUS0 register provides information regarding the last Catastrophic Save operation.

If Bit 0, SAVE_SUCCESS, is set to 1, the last Catastrophic Save operation completed without any errors.

If Bit 1, SAVE_ERROR, is set to 1, the last Catastrophic Save operation failed.

If Bit 4, ABORT_SUCCESS, is set to 1, the last Catastrophic Save operation was aborted by the Host. When the last Catastrophic Save operation is aborted, SAVE_ERROR shall also be set to 1.

If Bit 5, ABORT_ERROR, is set to 1, the abort of the last Catastrophic Save operation failed.

The module shall set this register to 0 when the Host requests to clear all status registers or clear the Save status register.

5) ERASE_STATUS0 – Offset 0x68

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : ERASE_SUCCESS [1] : ERASE_ERROR [3:2] : Reserved [4] : ABORT_SUCCESS [5] : ABORT_ERROR [7:6] : Reserved	RO	Y	N	0

The ERASE_STATUS0 register provides information regarding the last Erase operation.

If Bit 0, ERASE_SUCCESS, is set to 1, the last Erase operation completed without any errors.

If Bit 1, ERASE_ERROR, is set to 1, the last Erase operation failed.

If Bit 4, ABORT_SUCCESS, is set to 1, the last Erase operation was aborted by the Host. When the last Erase operation is aborted, ERASE_ERROR shall also be set to 1.

If Bit 5, ABORT_ERROR, is set to 1, the abort of the last Erase operation failed.

The module shall set this register to 0 when the Host requests to clear all status registers or clear the Erase status register.

6) FACTORY_DEFAULT_STATUS0 – Offset 0x6C

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : FACTORY_DEFAULT_SUCCESS [1] : FACTORY_DEFAULT_ERROR [7:2] : Reserved	RO	Y	N	0

The FACTORY_DEFAULT_STATUS0 register provides information regarding the last Factory Default operation.

If Bit 0, FACTORY_DEFAULT_SUCCESS, is set to 1, the last Factory Default operation completed without any errors.

If Bit 1, FACTORY_DEFAULT_ERROR, is set to 1, the last Factory Default operation failed. The state of the module after a failed Factory Default operation is non-deterministic.

The module shall set this register to 0 when the Host requests to clear all status registers or clear the Factory Default status register.

7) SET_EVENT_NOTIFICATION_STATUS0 – Offset 0x6E

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : SET_EVENT_NOTIFICATION_SUCCESS [1] : SET_EVENT_NOTIFICATION_ERROR [2] : PERSISTENCY_ENABLED [3] : WARNING_THRESHOLD_ENABLED [4] : Reserved [7:5] : Reserved	RO	Y	N	0

The SET_EVENT_NOTIFICATION_STATUS0 register provides information regarding the last Set Event Notification operation.

If Bit 0, SET_EVENT_NOTIFICATION_SUCCESS, is set to 1, the last Set Event Notification operation completed without any errors.

If Bit 1, SET_EVENT_NOTIFICATION_ERROR, is set to 1, the last Set Event Notification operation failed.

If Bit 2, PERSISTENCY_ENABLED, is set to 1, the module will generate an event notification when a loss of persistency or persistency restored event has been detected. If Bit 2 is set to 0, the module will not generate an event notification when a loss of persistency or persistency restored event has been detected.

If Bit 3, WARNING_THRESHOLD_ENABLED, is set to 1, the module will generate an event notification when a warning threshold has been exceeded or below warning threshold event has been detected. If Bit 3 is set to 0, the module will not generate an event notification when a warning threshold has been exceeded or below warning threshold event has been detected.

Bit 4 was VOLTAGE_REGULATOR_FAILED_ENABLED but is now a Reserved bit.

The module shall set SET_EVENT_NOTIFICATION_SUCCESS and SET_EVENT_NOTIFICATION_ERROR to 0 when the Host requests to clear all status registers or clear the Set Event Notification status register.

8) SET_ES_POLICY_STATUS – Offset 0x70

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : SET_ES_POLICY_SUCCESS [1] : SET_ES_POLICY_ERROR [2] : DEVICE_MANAGED_POLICY_ENABLED [3] : HOST_MANAGED_POLICY_ENABLED [7:4] : Reserved	RO	Y	N	0

The SET_ES_POLICY_STATUS register provides information regarding the last Set Energy Source Policy operation.

If Bit 0, SET_ES_POLICY_SUCCESS, is set to 1, the last Set Energy Source Policy operation completed without any errors.

If Bit 1, SET_ES_POLICY_ERROR, is set to 1, the last Set Energy Source Policy operation failed.

If Bit 2, DEVICE_MANAGED_POLICY_ENABLED, is set to 1, the module is configured to use a locally attached Energy Source and will monitor the health of the Energy Source. If Bit 2 is set to 1, Bit 3 shall be set to 0.

If Bit 3, HOST_MANAGED_POLICY_ENABLED, is set to 1, the module is configured to use the 12V pin as the Energy Source for the Catastrophic Save operation. If Bit 3 is set to 1, Bit 2 shall be set to 0.

The module shall set SET_ES_POLICY_SUCCESS and SET_ES_POLICY_ERROR to 0 when the Host requests to clear all status registers or clear the Set Energy Source Policy status register.

9) FIRMWARE_OPS_STATUS – Offset 0x71

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : FIRMWARE_OPS_SUCCESS [1] : FIRMWARE_OPS_ERROR [2] : FIRMWARE_UPDATE_MODE [3] : FIRMWARE_BLOCK_RECEIVED [4] : ABORT_SUCCESS [5] : ABORT_ERROR [7:6] : Reserved	RO	Y	N	0

The FIRMWARE_OPS_STATUS register provides information regarding the last Firmware Operations operation.

If Bit 0, FIRMWARE_OPS_SUCCESS, is set to 1, the last Firmware Operations operation completed without any errors.

If Bit 1, FIRMWARE_OPS_ERROR, is set to 1, the last Firmware Operations operation failed.

If Bit 2, FIRMWARE_UPDATE_MODE, is set to 1, the module is in the Firmware Update mode where firmware on the module can be changed. If Bit 2 is 0, firmware on the module cannot be change.

If Bit 3, FIRMWARE_BLOCK_RECEIVED, is set to 1, the last BLOCK has been received successfully by the NVDIMM and the host may proceed with sending another BLOCK.

If Bit 4, ABORT_SUCCESS, is set to 1, the last Firmware Operations operation was aborted by the Host. When the last Firmware Operations operation is aborted, FIRMWARE_OPS_ERROR shall also be set to 1.

If Bit 5, ABORT_ERROR, is set to 1, the abort of the last Firmware Operations operation failed.

The module shall set all bits in this register to 0 except Bit 2, FIRMWARE_UPDATE_MODE, when the Host requests to clear all status registers or clear the Firmware Operations status register.

10) OPERATIONAL_UNIT_OPS_STATUS – Offset 0x72

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : OPERATIONAL_UNIT_OPS_SUCCESS [1] : OPERATIONAL_UNIT_OPS_ERROR [2] : ENDURANCE_LIMIT_REACHED [5:3] : Reserved [6] : ABORT_SUCCESS [7] : ABORT_ERROR	RO	Y	N	0

The OPERATIONAL_UNIT_OPS_STATUS register provides information regarding the last Operational Unit Operations operation.

If Bit 0, OPERATIONAL_UNIT_OPS_SUCCESS, is set to 1, the last Operational Unit Operations operation completed without any errors.

If Bit 1, OPERATIONAL_UNIT_OPS_ERROR, is set to 1, the last Operational Unit Operations operation failed.

If Bit 2, ENDURANCE_LIMIT_REACHED, is set to 1, the Set Operational Unit operation failed due to the module reaching the endurance limit of the media.

If Bit 6, ABORT_SUCCESS, is set to 1, the last Operational Unit Operations operation was aborted by the Host. When the last Operational Unit Operations operation is aborted, OPERATIONAL_UNIT_OPS_ERROR shall also be set to 1.

If Bit 7, ABORT_ERROR, is set to 1, the abort of the last Operational Unit Operations operation failed.

The module shall set all bits in this register to 0 when the Host requests to clear all status registers or clear the Operational Unit Operations status register.

B.2.1.6 Catastrophic Save Registers

The registers in this section provide Catastrophic Save related information.

1) CSAVE_INFO0 – Offset 0x80

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : NVM_Data_Valid. Only valid if the SAVE_STATUS0 register SAVE_STATUS bit is set to 1. [1] : START_SAVE_CMD [2] : SAVE_N [7:3] : Reserved	RO	Y	Y	0

The CSIZE_INFO0 register provides information on whether there is a valid data in the NVM subsystem and the trigger source of the last Catastrophic Save operation.

If Bit 0, NVM_Data_Valid, is set, module has a valid data in the NVM subsystem. Bit 0 value is valid only if the SAVE_STATUS0 register SAVE_STATUS bit is set to 1.

If Bit 1, START_SAVE_CMD, is set, the last Catastrophic Save operation was initiated through the START_SAVE bit in the NVDIMM_FUNC_CMD0 register.

If Bit 2, SAVE_N, is set, the last Catastrophic Save operation was initiated by the SAVE_N pin.

2) CSAVE_FAIL_INFO0 – Offset 0x84

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : VOLTAGE_REGULATOR_FAILED	RO	Y	Y	0
[1] : VDD_LOST				
[2] : VPP_LOST				
[3] : VTT_LOST				
[4] : Reserved				
[5] : CONTROLLER_HARDWARE_ERROR				
[6] : Reserved				
[7] : NVM_MEDIA_ERROR				

The CSAVE_FAIL_INFO0 register provides failure information of the last Catastrophic Save operation.

If Bit 0, VOLTAGE_REGULATOR_FAILED, is set, the last Catastrophic Save operation failed due to the module detecting a voltage regulator failure.

If Bit 1, VDD_LOST, is set, the last Catastrophic Save operation failed due to the module detecting a lost Vdd condition.

If Bit 2, VPP_LOST, is set, the last Catastrophic Save operation failed due to the module detecting a lost Vpp condition.

If Bit3, VTT_LOST, is set, the last Catastrophic Save operation failed due to the module detecting a lost Vtt condition.

If Bit 4, Reserved.

If Bit 5, CONTROLLER_HARDWARE_ERROR, is set, the last Catastrophic Save operation failed due to the module encountering a controller hardware error.

If Bit 6, Reserved

If Bit 7, NVM_MEDIA_ERROR, is set, the last Catastrophic Save operation failed due to the module encountering a non-volatile media error.

More than one bit can be set in CSAVE_FAIL_INFO0 and CSAVE_FAIL_INFO1 registers.

3) CSAVE_FAIL_INFO1 – Offset 0x85

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : NOT_ENOUGH_ENERGY_FOR_CSAVE	RO	Y	Y	0
[1] : PARTIAL_DATA_SAVED				
[2] : SAVE_ABORT				
[3] : NO_SAVE_N				
[4] : INSUFFICIENT_SAVE_N				
[7:5] : Reserved				

The CSAVE_FAIL_INFO1 register provides failure information of the last Catastrophic Save operation.

If Bit 0, NOT_ENOUGH_ENERGY_FOR_CSAVE, is set, the last Catastrophic Save operation failed due to the module detecting there is not enough energy for a Catastrophic Save operation. This bit is set only if module is in Device Managed Policy.

If Bit 1, PARTIAL_DATA_SAVED, is set, not all of the SDRAM data was saved during the last Catastrophic Save operation.

If Bit 2, SAVE_ABORT, is set, the last Catastrophic Save operation was aborted by the host.

If Bit 3, NO_SAVE_N, is set, no Catastrophic Save operation was started as the module did not detect an asserted SAVE_N.

If Bit 4, INSUFFICIENT_SAVE_N, is set, a Catastrophic Save was not initiated due to insufficient number of SAVE_N pulse(s).

More than one bit can be set in CSAVE_FAIL_INFO0 and CSAVE_FAIL_INFO1 registers.

B.2.1.7 Thresholds Registers

The registers in this section are related to the thresholds support provided by the module.

1) NVM_LIFETIME_ERROR_THRESHOLD – Offset 0x90

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : NVM lifetime percentage error threshold	RO	Y	Y	Non-zero value

The NVM_LIFETIME_ERROR_THRESHOLD register provides the non-volatile memory lifetime percentage value at which the lifetime of the non-volatile memory subsystem has exceeded its warranty. The threshold is in 1% granularity.

2) ES_LIFETIME_ERROR_THRESHOLD – Offset 0x91

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : ES lifetime percentage error threshold	RO	N	Y	Implementation-specific

The ES_LIFETIME_ERROR_THRESHOLD register provides the Energy Source lifetime percentage value at which the lifetime of the Energy Source has exceeded its warranty. This register is mandatory if module is configured for Device Managed Policy. The threshold is in 1% granularity.

For modules configured for Host Managed Policy, the module shall return the value 0.

3) ES_TEMP_ERROR_THRESHOLD – Offset 0x92

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : ES temperature error threshold	RO	N	Y	Implementation-specific

The ES_TEMP_ERROR_THRESHOLD register provides the Energy Source temperature value in Celsius at which the Energy Source has exceeded its warranty. The minimum value is 0. This register is mandatory if module is configured for Device Managed Policy. The threshold is in 1 degree Celsius granularity.

For modules configured for Host Managed Policy, the module shall return the value 0.

4) NVM_LIFETIME_WARNING_THRESHOLD – Offset 0x98

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : NVM lifetime percentage warning threshold	RW	Y	Y	Non-zero value

The NVM_LIFETIME_WARNING_THRESHOLD register provides the warning threshold for the non-volatile memory lifetime percentage value. The value of this register shall be greater than NVM_LIFETIME_ERROR_THRESHOLD register. If the Host attempts to set this register to a value that is less than or equal to NVM_LIFETIME_ERROR_THRESHOLD, the module shall not change this register value. The threshold is in 1% granularity.

5) ES_LIFETIME_WARNING_THRESHOLD – Offset 0x99

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : ES lifetime percentage warning threshold	RW	N	Y	Implementation-specific

The ES_LIFETIME_WARNING_THRESHOLD register provides the warning threshold for the Energy Source lifetime percentage value. The value of this register shall be greater than ES_LIFETIME_ERROR_THRESHOLD register. If the Host attempts to set this register to a value that is less than or equal to ES_LIFETIME_ERROR_THRESHOLD, the module shall not change this register value. This register is mandatory if module is configured for Device Managed Policy. The threshold is in 1% granularity.

For modules configured for Host Managed Policy, the module shall return the value 0.

6) ES_TEMP_WARNING_THRESHOLD – Offset 0x9A

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : ES temperature warning threshold	RW	N	Y	Implementation-specific

The ES_TEMP_WARNING_THRESHOLD register provides the warning threshold for the Energy Source temperature value. The value of this register shall be less than ES_TEMP_ERROR_THRESHOLD register. If the Host attempts to set this register to a value that is greater than or equal to ES_TEMP_ERROR_THRESHOLD, the module shall not change this register value. This register is mandatory if module is configured for Device Managed Policy. The threshold is in 1 degree Celsius granularity.

For modules configured for Host Managed Policy, the module shall return the value 0.

B.2.1.8 Module Registers

The registers in this section provide module related information.

1) MODULE_HEALTH – Offset 0xA0

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : PERSISTENCY_LOST_ERROR	RO	Y	N	0
[1] : WARNING_THRESHOLD_EXCEEDED				
[2] : PERSISTENCY_RESTORED				
[3] : BELOW_WARNING_THRESHOLD				
[4] : PERMANENT_HARDWARE_FAILURE				
[5] : EVENT_N_LOW				
[7:6] : Reserved				

The MODULE_HEALTH register provides a high level status register that the Host can read to determine if there are issues with the module.

If Bit 0, PERSISTENCY_LOST_ERROR, is set, this indicates that the module is not capable of persisting data during the Catastrophic Save operation. This bit shall be a logical OR of all defined bits from the MODULE_HEALTH_STATUS0, MODULE_HEALTH_STATUS1 and ERROR_THRESHOLD_STATUS registers.

If Bit 1, WARNING_THRESHOLD_EXCEEDED, is set, this indicates that one or more warning threshold exceeded events have been detected. This bit shall be a logical OR of all defined bits from the WARNING_THRESHOLD_STATUS register.

If Bit 2, PERSISTENCY_RESTORED, is set, this indicates that the previous condition(s) causing the module to be not capable of persisting data during the Catastrophic Save operation is not present and the module is capable of persisting data during the Catastrophic Save operation.

If Bit 3, BELOW_WARNING_THRESHOLD, is set, this indicates that a previous warning threshold exceeded threshold no longer occurs.

If Bit 4, PERMANENT_HARDWARE_FAILURE, is set, this indicates that the module has a permanent hardware failure and module replacement is needed.

If Bit 5, EVENT_N_LOW, is set, this indicates that the module is driving the EVENT_N pin low on DDR bus.

2) MODULE_HEALTH_STATUS0 – Offset 0xA1

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : VOLTAGE_REGULATOR_FAILED	RO	Y	N	0
[1] : VDD_LOST				
[2] : VPP_LOST				
[3] : VTT_LOST				
[4] : Reserved				
[5] : CONTROLLER_HARDWARE_ERROR				
[6] : Reserved				
[7] : NVM_LIFETIME_ERROR				

The MODULE_HEALTH_STATUS0 register provides more detailed information regarding the module health.

If Bit 0, VOLTAGE_REGULATOR_FAILED, is set, the controller has detected a voltage regulator failure.

If Bit 1, VDD_LOST, is set, the module has encountered an error on operational voltage regulator output. If voltage regulator is turned OFF, then module does not set this bit.

If Bit 2, VPP_LOST, is set, the module has encountered an error on operational voltage regulator output. If voltage regulator is turned OFF, then module does not set this bit.

If Bit 3, VTT_LOST, is set, the module has encountered an error on operational voltage regulator output. If voltage regulator is turned OFF, then module does not set this bit.

If Bit 4, Reserved

If Bit 5, CONTROLLER_HARDWARE_ERROR is set, the module has detected a controller hardware error that causes data persistency to be lost.

If Bit 6, Reserved

If Bit 7, NVM_LIFETIME_ERROR, is set, the module has detected a non-volatile memory lifetime error.

3) MODULE_HEALTH_STATUS1 – Offset 0xA2

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : NOT_ENOUGH_ENERGY_FOR_CSAVE	RO	Y	N	0
[1] : INVALID_FIRMWARE_ERROR				
[2] : Reserved				
[3] : NO_ES_PRESENT				
[4] : ES_POLICY_NOT_SET				
[5] : ES_HARDWARE_FAILURE				
[6] : ES_HEALTH_ASSESSMENT_ERROR				
[7:] : Reserved				

The MODULE_HEALTH_STATUS1 register provides more detailed information regarding the module health.

If Bit 0, NOT_ENOUGH_ENERGY_FOR_CSAVE, is set, the module has detected that the Energy Source does not have enough energy to support a Catastrophic Save operation. This bit shall only be set when the module is in Device Managed Policy mode. This is only valid when the NVDIMM-P requires the Energy Source.

If Bit 1, INVALID_FIRMWARE_ERROR is set, the module has detected an invalid firmware during initialization. The invalid firmware could be due to image corruption or a wrong firmware image.

If Bit 2, Reserved

If Bit 3, NO_ES_PRESENT, is set, the module has detected that there is no Energy Source. When configured to run in Device Managed Policy, this bit shall be set if there is Energy Source attached to the module. In Host Managed Policy, this bit shall be set if the module does not detect any power on the 12V pin.

If Bit 4, ES_POLICY_NOT_SET, is set, the Energy Source policy has not been set on the module.

If Bit 5, ES_HARDWARE_FAILURE, is set, the module has detected that the attached Energy Source has failed due to a hardware error. This bit shall only be set when the module is in Device Managed Policy mode.

If Bit 6, ES_HEALTH_ASSESSMENT_ERROR, is set, the module has encountered an error while trying to assess the health of the attached Energy Source. This bit shall only be set when the module is in Device Managed Policy mode.

4) ERROR_THRESHOLD_STATUS – Offset 0xA5

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : NVM_LIFETIME_ERROR [1] : ES_LIFETIME_ERROR [2] : ES_TEMP_ERROR [7:3] : Reserved	RO	Y	N	0

The ERROR_THRESHOLD_STATUS register provides status regarding the error thresholds on the modules. If a bit is set, this indicates that the error threshold has been met or exceeded. If the current value exceeds both the error and warning thresholds, only the error threshold bit shall be set. This is only valid when the NVDIMM-P requires the Energy Source.

If Bit 0, NVM_LIFETIME_ERROR, is set, the module has detected that the non-volatile memory lifetime is either at or exceeds the error threshold. If bit is clear, the non-volatile memory lifetime is below the error threshold.

If Bit 1, ES_LIFETIME_ERROR, is set, the module has detected that the Energy Source lifetime is either at or exceeds the error threshold. If bit is clear, the Energy Source lifetime is below the error threshold.

If Bit 2, ES_TEMP_ERROR, is set, the module has detected that the Energy Source temperature is either at or exceeds the error threshold. If bit is clear, the Energy Source temperature is below the error threshold.

5) WARNING_THRESHOLD_STATUS – Offset 0xA7

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : NVM_LIFETIME_WARNING [1] : ES_LIFETIME_WARNING [2] : ES_TEMP_WARNING [7:3] : Reserved	RO	Y	N	0

The WARNING_THRESHOLD_STATUS register provides status regarding the warning thresholds on the modules. If a bit is set, this indicates that the warning threshold has been met or exceeded. If the current value exceeds both the error and warning thresholds, only the error threshold bit shall be set. This is only valid when the NVDIMM-P requires the Energy Source.

If Bit 0, NVM_LIFETIME_WARNING, is set, the module has detected that the non-volatile memory lifetime is either at or exceeds the warning threshold. If bit is clear, the non-volatile memory lifetime is below the warning threshold.

If Bit 1, ES_LIFETIME_WARNING, is set, the module has detected that the Energy Source lifetime is either at or exceeds the warning threshold. If bit is clear, the Energy Source lifetime is below the warning threshold.

If Bit 2, ES_TEMP_WARNING, is set, the module has detected that the Energy Source temperature is either at or exceeds the warning threshold. If bit is clear, the Energy Source temperature is below the warning threshold.

6) AUTO_ES_HEALTH_FREQUENCY – Offset 0xA9

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[2:0] : Value in days [7:3] : Value in weeks	RW	N	Y	>= 1

The AUTO_ES_HEALTH_FREQUENCY register provides the current frequency of the Energy Source health assessment done by the module. This register shall be supported when the module is in Device Managed Policy mode. When module is in Host Managed Policy mode, the module shall return the value 0.

The minimum value supported is 1 day. Module need to be running for the time period in this register before the first Energy Source health check is done. If this register is written to, the new value is used at the next Energy Source health check.

NOTE An Energy Source health check may have an effect on the longevity of the Energy Source device.

7) MODULE_OPS_CONFIG – Offset 0xAA

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : SAVE_N_LOW_DURING_CSAVE [2:1] : SAVE_N Assertion Mode -00: Default Mode (Single-pulse Trigger) -01: Two-pulse Trigger Mode -10: Three-pulse Trigger Mode -11: Reserved [3] : LCOM_ENABLE [7:4] : Reserved	RW	Y	N	0

The MODULE_OPS_CONFIG register provides ability to configure the operational behavior of the module. The Host uses this register to adjust the behavior of the module from the default behavior.

If Bit 0, SAVE_N_LOW_DURING_CSAVE, is set, the module shall drive the SAVE_N pin low during the duration of the Catastrophic Save operation. The default behavior of the module is to not drive the SAVE_N pin low during Catastrophic Save.

If Bits[2:1], SAVE_N Assertion Mode, are set to 00b, the module initiates Catastrophic Save operation within 1 usec after the SAVE_N pin is taken low. The NV controller must disconnect the module from the platform command/address bus once SAVE_N is detected Low (i.e., within 1 usec from SAVE_N going low) since those signals are not guaranteed to be valid after that point.

If Bits[2:1], SAVE_N Assertion Mode, are set to 01b and Two-pulse SAVE_N Trigger Mode Supported in CAPABILITIES (Offset 0x10 Bit 5) is set, the first time when SAVE_N signal is pulsed Low indicates an early warning of an impending Catastrophic Save event due to power failure detection by the system. When SAVE_N signal is pulsed Low a second time, the module initiates Catastrophic Save operation within 1 usec from the start of the second low pulse. The NV controller must disconnect the module from the platform command/address bus once SAVE_N is detected Low for a second time (i.e., within 1 usec from the start of the second low pulse) since those signals are not guaranteed to be valid after that point. In order to use Two-pulse SAVE_N Trigger Mode in platforms

where two or more modules use a shared SAVE_N signal, the Host controller is required to configure the NVDIMMs properly so that the modules do not falsely trigger Save events in any of the modules connected to the same SAVE_N net. This restriction does not apply to systems where each NVDIMM module has a dedicated SAVE_N signal in the platform.

If Bits[2:1], SAVE_N Assertion Mode, are set to 10b and Three-pulse SAVE_N Trigger Mode Supported in CAPABILITIES (Offset 0x10 Bit 6) is set, the first time when SAVE_N signal is pulsed Low indicates an early warning of an impending Catastrophic Save event due to power failure detection by the system. When SAVE_N signal is pulsed Low a second time, the media controller must disconnect the module from the platform command/address bus once SAVE_N is detected Low for a second time (i.e., within 1 usec from the start of the second low pulse) since those signals are not guaranteed to be valid after that point. When SAVE_N signal is pulsed Low a third time, the module initiates Catastrophic Save operation within 1 usec from the start of the third low pulse. In order to use Three-pulse SAVE_N Trigger Mode in platforms where two or more modules use a shared SAVE_N signal, the Host controller is required to configure the NVDIMMs properly so that the modules do not falsely trigger Catastrophic Save events in any of the modules connected to the same SAVE_N net. This restriction does not apply to systems where each NVDIMM module has a dedicated SAVE_N signal in the platform.

Table 133 - Timing

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{SAVE_PW_LOW}}$	SAVE_N Pulse Width LOW Duration	1	-	-	μs
$t_{\text{SAVE_PW_HIGH}}$	SAVE_N Pulse Width HIGH Duration	1	-	-	μs
$t_{\text{SRE_Hold}}$	Hold Time after end of SAVE_N pulse	25	-	-	μs

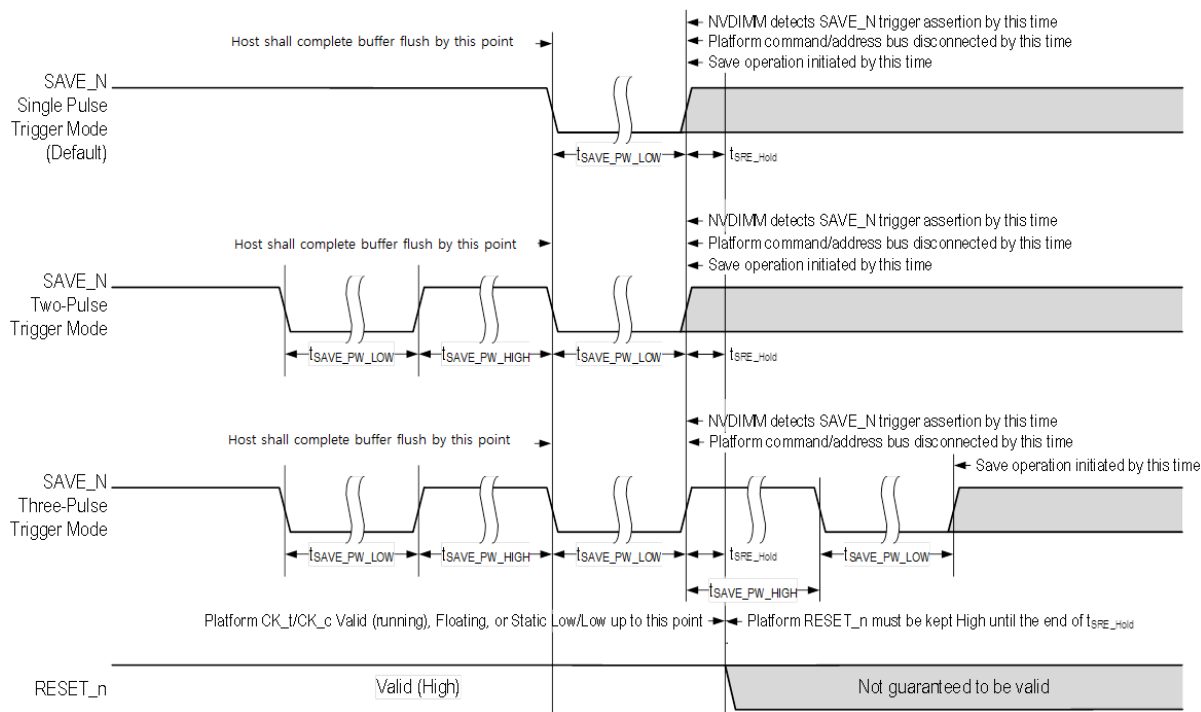


Figure 35 - SAVE_N trigger mode timing diagram.

If Bit 3, LCOM_ENABLE, is set, the LCOM interface is enabled.

B.2.1.9 NVM Subsystem Registers

The registers in this section provide NVM subsystem related information.

1) NVM_LIFETIME – Offset 0xC0

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : NVM lifetime percentage from 0 to 100.	RO	Y	Y	Non-zero value

The NVM_LIFETIME register provides the last known non-volatile memory lifetime percentage value. The percentage value shall be from 0 to 100 where 100 represents a healthy state. The NVM_LIFETIME register is not impacted by the Factory Default operation.

B.2.1.10 Write Data Retire Policy

1) WRITE_DATA_POLICY – Offset 0x90

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7] XWRITE data retire policy	RW	N	N	
[6] PWRITE data retire policy				
[5:0] Reserved				

If Bit 7 is 0, XWRITE data stored in cache or buffer will be processed as Write Back cache data to the non-volatile memory media. If it is 1, then the data will be processed as Write Through policy.

If Bit 6 is 0, PWRITE data stored in cache or buffer will be processed as Write Back cache data to the non-volatile memory media. If it is 1, then the data will be processed as Write Through policy.

B.2.1.11 CSAVE_POWER_REQ_x

1) CSAVE_POWER_REQ_A0 – Offset 0x80

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Average power required for Catastrophic Save operation in milliwatts LSB.	RO	N	Y	Implementation-specific

2) CSAVE_POWER_REQ_A1 – Offset 0x81

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Average power required for Catastrophic Save operation in milliwatts MSB.	RO	N	Y	Implementation-specific

The CSAVE_POWER_REQ_A0~1 registers provide the average power(milliwatts) required for WT(Write Through) mode PWRITE data in the Catastrophic Save operation.

For a Host that uses shared Energy Source, Host should use the CSAVE_POWER_REQ_A0 and CSAVE_POWER_REQ_A1 register values for energy budgeting. The energy required is calculated by multiplying the CSAVE_TIMEOUT_A0 and CSAVE_TIMEOUT_A1 register values by the CSAVE_POWER_REQ_A0 and CSAVE_POWER_REQ_A1 register values.

This register shall be supported if the module supports Host Managed Policy.

3) CSAVE_POWER_REQ_B0 – Offset 0x82

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Average power required for Catastrophic Save operation in milliwatts LSB.	RO	N	Y	Implementation-specific

4) CSAVE_POWER_REQ_B1 – Offset 0x83

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Average power required for Catastrophic Save operation in milliwatts MSB.	RO	N	Y	Implementation-specific

The CSAVE_POWER_REQ_A0~1 registers provide the average power(milliwatts) required for WB(Write Back) mode PWRITE data in the Catastrophic Save operation.

For a Host that uses shared Energy Source, Host should use the CSAVE_POWER_REQ_B0 and CSAVE_POWER_REQ_B1 register values for energy budgeting. The energy required is calculated by multiplying the CSAVE_TIMEOUT_B0 and CSAVE_TIMEOUT_B1 register values by the CSAVE_POWER_REQ_B0 and CSAVE_POWER_REQ_B1 register values.

This register shall be supported if the module supports Host Managed Policy.

5) CSAVE_POWER_REQ_C0 – Offset 0x84

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Average power required for Catastrophic Save operation in milliwatts LSB.	RO	N	Y	Implementation-specific

6) CSAVE_POWER_REQ_C1 – Offset 0x85

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Average power required for Catastrophic Save operation in milliwatts MSB.	RO	N	Y	Implementation-specific

The CSAVE_POWER_REQ_C0~1 registers provide the average power(milliwatts) required for WT(Write Through) mode PWRITE and XWRITE data in the Catastrophic Save operation.

For a Host that uses shared Energy Source, Host should use the CSAVE_POWER_REQ_C0 and CSAVE_POWER_REQ_C1 register values for energy budgeting. The energy required is calculated by multiplying the CSAVE_TIMEOUT_C0 and CSAVE_TIMEOUT_C1 register values by the CSAVE_POWER_REQ_C0 and CSAVE_POWER_REQ_C1 register values.

This register shall be supported if the module supports Host Managed Policy.

7) CSAVE_POWER_REQ_D0 – Offset 0x86

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Average power required for Catastrophic Save operation in milliwatts LSB.	RO	N	Y	Implementation-specific

8) CSAVE_POWER_REQ_D1 – Offset 0x87

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Average power required for Catastrophic Save operation in milliwatts MSB.	RO	N	Y	Implementation-specific

The CSAVE_POWER_REQ_A0~1 registers provide the average power(milliwatts) required for WB(Write Back) mode PWRITE and XWRITE data in the Catastrophic Save operation.

For a Host that uses shared Energy Source, Host should use the CSAVE_POWER_REQ_D0 and CSAVE_POWER_REQ_D1 register values for energy budgeting. The energy required is calculated by multiplying the CSAVE_TIMEOUT_D0 and CSAVE_TIMEOUT_D1 register values by the CSAVE_POWER_REQ_D0 and CSAVE_POWER_REQ_D1 register values.

This register shall be supported if the module supports Host Managed Policy.

B.2.1.12 CSAVE_TIMEOUT_Exx

1) CSAVE_TIMEOUT_A0 – Offset 0x88

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Worst case Catastrophic Save completion latency LSB	RO	Y	Y	Implementation-specific

2) CSAVE_TIMEOUT_A1 – Offset 0x89

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[6:0] : Worst case Catastrophic Save completion latency MSB [7] : 0 – Indicates completion latency value is in units of milliseconds. 1 – Indicates completion latency value is in units of seconds.	RO	Y	Y	Implementation-specific

The CSAVE_TIMEOUT_A0~1 registers provide the Catastrophic Save completion latency in milliseconds or seconds for WT(Write Through) mode PWRITE data retire.

If Bit 7 is 0 at CSAVE_TIMEOUT_A1, the worst case completion latency value is in units of milliseconds. If Bit 7 is 1, the worst case completion latency value is in units of seconds.

3) CSAVE_TIMEOUT_B0 – Offset 0x8A

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Worst case Catastrophic Save completion latency LSB	RO	Y	Y	Implementation-specific

4) CSAVE_TIMEOUT_B1 – Offset 0x8B

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
<p>[6:0] : Worst case Catastrophic Save completion latency MSB</p> <p>[7] : 0 – Indicates completion latency value is in units of milliseconds.</p> <p>1 – Indicates completion latency value is in units of seconds.</p>	RO	Y	Y	Implementation-specific

The CSAVE_TIMEOUT_B0~1 registers provide the Catastrophic Save completion latency in milliseconds or seconds for WB(Write Back) mode PWRITE data retire.

If Bit 7 is 0 at CSAVE_TIMEOUT_B1, the worst case completion latency value is in units of milliseconds. If Bit 7 is 1, the worst case completion latency value is in units of seconds.

5) CSAVE_TIMEOUT_C0 – Offset 0x8C

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Worst case Catastrophic Save completion latency LSB	RO	Y	Y	Implementation-specific

6) CSAVE_TIMEOUT_C1 – Offset 0x8D

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
<p>[6:0] : Worst case Catastrophic Save completion latency MSB</p> <p>[7] : 0 – Indicates completion latency value is in units of milliseconds.</p> <p>1 – Indicates completion latency value is in units of seconds.</p>	RO	Y	Y	Implementation-specific

The CSAVE_TIMEOUT_C0~1 registers provide the Catastrophic Save completion latency in milliseconds or seconds for WT(Write Through) mode PWRITE and XWRITE data retire.

If Bit 7 is 0 at CSAVE_TIMEOUT_C1, the worst case completion latency value is in units of milliseconds. If Bit 7 is 1, the worst case completion latency value is in units of seconds.

7) CSAVE_TIMEOUT_D0 – Offset 0x8E

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Worst case Catastrophic Save completion latency LSB	RO	Y	Y	Implementation-specific

8) CSAVE_TIMEOUT_D1 – Offset 0x8F

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
<p>[6:0] : Worst case Catastrophic Save completion latency MSB</p> <p>[7] : 0 – Indicates completion latency value is in units of milliseconds.</p> <p>1 – Indicates completion latency value is in units of seconds.</p>	RO	Y	Y	Implementation-specific

The CSAVE_TIMEOUT_D0~1 registers provide the Catastrophic Save completion latency in milliseconds or seconds for WB(Write Back) mode PWRITE and XWRITE data retire.

If Bit 7 is 0 at CSAVE_TIMEOUT_D1, the worst case completion latency value is in units of milliseconds. If Bit 7 is 1, the worst case completion latency value is in units of seconds.

B.2.2 Page 1 Register Map (Energy Source)

The registers in page 1 are related to Energy Source and organized based on categories. This page is mandatory when the module is in Device Managed Policy mode. When module is in Host Managed Policy mode, the module shall not allow a page switch to this page. Table 6 shows the layout of the categories in page 1.

Table 134 - Page 1 categories

Offset	Category	Description
0x00 – 0x03	Paging Mechanism	Registers related to I ² C page support.
0x04 – 0x0F	Energy Source Version	Registers providing Energy Source version information.
0x10 – 0x2F	Energy Source Characteristics	Registers providing Energy Source characteristics information.
0x30 – 0x4F	Energy Source Runtime Command	Registers related to Energy Source runtime commands.
0x50 – 0x6F	Energy Source Runtime Command Status	Registers providing Energy Source runtime command status information.
0x70 – 0xFF	Energy Source	Registers providing Energy Source related information.

Table 7 shows the registers that are in page 1.

Table 135 - Page 1 register map

Offset	Register Name	Host Access Property	Mandatory	Persistent Across Power Cycles
0x00	OPEN_PAGE	RW	Y	N
0x01–0x03	Reserved			
0x04	ES_HWREV	RO	N	Y
0x05	Reserved			
0x06	ES_FWREV0	RO	N	Y
0x07	ES_FWREV1	RO	N	Y
0x08–0x0F	Reserved			
0x10	ES_CHARGE_TIMEOUT0	RO	N	Y
0x11	ES_CHARGE_TIMEOUT1	RO	N	Y
0x12	MIN_ES_OPERATING_TEMP	RO	N	Y
0x13	MAX_ES_OPERATING_TEMP	RO	N	Y
0x14	ES_ATTRIBUTES	RO	N	Y
0x15	ES_TECH	RO	N	Y
0x16–0x2F	Reserved			
0x30	ES_FUNC_CMD0	WO	N	N
0x31–0x4F	Reserved			
0x50	ES_CMD_STATUS0	RO	N	N
0x51–0x6F	Reserved			
0x70	ES_LIFETIME	RO	N	N
0x71	ES_TEMP0	RO	N	N
0x72	ES_TEMP1	RO	N	N
0x73	ES_RUNTIME0	RO	N	Y
0x74	ES_RUNTIME1	RO	N	Y
0x75–0xFF	Reserved			

B.2.2.1 Paging Mechanism Registers

The registers in this section are related to the I²C paging mechanism supported by the module.

1) OPEN_PAGE – Offset 0x00

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Open page number	RW	Y	N	0

When the OPEN_PAGE register is read, it returns the current opened page number. When the OPEN_PAGE register is written to, the module shall attempt to set the current opened page number to the value written. The default value of OPEN_PAGE shall be 0.

B.2.2.2 Energy Source Version Registers

The registers in this section provide Energy Source version information.

1) ES_HWREV – Offset 0x04

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Energy source hardware revision	RO	N	Y	Implementation-specific

The ES_HWREV register returns the Energy Source hardware revision.

2) ES_FWREV0 – Offset 0x6

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Energy source firmware revision LSB	RO	N	Y	Implementation-specific

The ES_FWREV0 register returns the least significant byte of the Energy Source firmware revision.

The combination of the values returned by ES_FWREV0 and ES_FWREV1 shall be non-zero. Energy source firmware revision value shall be assigned in increasing order so that a larger revision value represents a more recent firmware image.

3) ES_FWREV1 – Offset 0x07

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Energy source firmware revision MSB	RO	N	Y	Implementation-specific

The ES_FWREV1 register returns the most significant byte of the Energy Source firmware revision.

The combination of the values returned by ES_FWREV0 and ES_FWREV1 shall be non-zero. Energy source firmware revision value shall be assigned in increasing order so that a larger revision value represents a more recent firmware image.

B.2.2.3 Energy Source Characteristics Registers

The registers in this section provide Energy Source characteristics information.

1) ES_CHARGE_TIMEOUT0 – Offset 0x10

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Worst case Energy Source charge time LSB	RO	N	Y	Implementation-specific

The ES_CHARGE_TIMEOUT0 returns the least significant byte of the worst case Energy Source charge time in seconds. The combination of ES_CHARGE_TIMEOUT0 and ES_CHARGE_TIMEOUT1 shall be non-zero.

2) ES_CHARGE_TIMEOUT1 – Offset 0x11

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Worst case Energy Source charge time MSB	RO	N	Y	Implementation-specific

The ES_CHARGE_TIMEOUT1 returns the most significant byte of the worst case Energy Source charge time in seconds. The combination of ES_CHARGE_TIMEOUT0 and ES_CHARGE_TIMEOUT1 shall be non-zero.

3) MIN_ES_OPERATING_TEMP – Offset 0x12

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Minimum Energy Source operating temperature	RO	N	Y	Implementation-specific

The MIN_ES_OPERATING_TEMP register returns the minimum operating temperature of the Energy Source in Celsius. The minimum value supported shall be 0.

4) MAX_ES_OPERATING_TEMP – Offset 0x13

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Maximum Energy Source operating temperature	RO	N	Y	Implementation-specific

The MAX_ES_OPERATING_TEMP register returns the maximum operating temperature of the Energy Source in Celsius.

5) ES_ATTRIBUTES – Offset 0x14

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : On Module [1] : Tethered [2] : Shared [7:3] Reserved	RO	N	Y	Non-zero value

The ES_ATTRIBUTES register provides attributes regarding the Energy Source. A set bit indicates that the Energy Source has the corresponding attribute. One or more bits may be set.

If Bit 0, On Module, is set, this indicates that there is an Energy Source on the module.

If Bit 1, Tethered, is set, this indicates that there is an Energy Source tethered to the module.

If Bit 2, Shared, is set, this indicates that the Energy Source is used by more than one module.

6) ES_TECH – Offset 0x15

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Undefined [1] : Supercapacitor [2] : Battery [3] : Hybrid capacitor [7:4] Reserved	RO	N	Y	Non-zero value

The ES_TECH register provides the technology used in the Energy Source. A set bit indicates that the corresponding technology is used in the Energy Source. One or more bits may be set.

If Bit 0, Undefined, is set, this indicates that the technology used in the Energy Source is not defined in this spec.

If Bit 1, Supercapacitor, is set, this indicates that the Energy Source uses supercapacitor.

If Bit 2, Battery, is set, this indicates that the Energy Source uses battery.

If Bit 3, Hybrid capacitor, is set, this indicates that the Energy Source uses hybrid capacitor.

B.2.2.4 Energy Source Runtime Command Registers

The registers in this section are related to Energy Source runtime commands.

1) ES_FUNC_CMD0 – Offset 0x30

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : MANUAL_ES_HEALTH_CHECK [1] : CL_ES_CMD_STATUS0 [7-1] : Reserved	WO	N	N	N/A

The ES_FUNC_CMD0 register allows a Host to initiate Energy Source runtime related commands. Only a bit in this register can be set. If more than 1 bit is set, module shall ignore the Host issued request.

If Bit 0, MANUAL_ES_HEALTH_CHECK, is set, the module shall initiate a health check of the Energy Source if there is no other Energy Source health check currently running. If there is a currently running Energy Source health check, module shall ignore the request. On receipt of this write and at completion of the health check, module shall update the ES_CMD_STATUS0 register.

If Bit 1, CL_ES_CMD_STATUS0, is set, the module shall set ES_CMD_STATUS0 register to 0.

B.2.2.5 Energy Source Runtime Command Status Registers

The registers in this section provide Energy Source runtime command status information.

1) ES_CMD_STATUS0 – Offset 0x50

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Health Check in Progress [1] : Health Check Succeeded [2] : Health Check Failed [3] : 0 - Automatic Health Check 1 - Manual Health Check [7:4] : Reserved	RO	N	N	0

The ES_CMD_STATUS0 register provides status information regarding the status of the Energy Source health check operation. Only a bit can be set for Bits 0 to 2.

If Bit 0, Health Check in Progress, is set, the module is executing an Energy Source health check operation.

If Bit 1, Health Check Succeeded, is set, the module has successfully completed an Energy Source health check.

If Bit 2, Health Check Failed, is set, the last Energy Source health check executed by the module failed.

If Bit 3 is set to 0, the currently running or last completed Energy Source health check operation was an automatic health check. If Bit 3 is set to 1, the currently running or last completed Energy Source health check operation was manually initiated.

B.2.2.6 Energy Source Registers

The registers in this section provide Energy Source related information.

1) ES_LIFETIME – Offset 0x70

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Energy source lifetime percentage from 0 to 100	RO	N	N	Non-zero value

The ES_LIFETIME register provides the last known Energy Source lifetime percentage from 0 to 100. 100 represents a healthy state. If no health check has been done yet, this register shall return the value 0xFF. The ES_LIFETIME register is not impacted by the Factory Default operation.

2) ES_TEMP0 – Offset 0x71

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Energy source temperature LSB	RO	N	N	Environment-specific

The ES_TEMP0 register provides the LSB of the last known Energy Source temperature in Celsius. The minimum value is 0. The temperature measurement frequency is implementation specific. If no Energy Source temperature measurement has been done yet or the module does not support measurement of Energy Source temperature, this register shall return the value 0xFF. The ES_TEMP0 register is not impacted by the Factory Default operation.

3) ES_TEMP1 – Offset 0x72

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Energy source temperature MSB	RO	N	N	Environment-specific

The ES_TEMP1 register provides the MSB of the last known Energy Source temperature in Celsius. The temperature measurement frequency is implementation specific. If no Energy Source temperature measurement has been done yet or the module does not support measurement of Energy Source temperature, this register shall return the value 0xFF. The ES_TEMP1 register is not impacted by the Factory Default operation.

4) ES_RUNTIME0 – Offset 0x73

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Total Energy Source runtime since manufacturing date LSB	RO	N	Y	0

The ES_RUNTIME0 register returns the least significant byte of the time the Energy Source has been operational since the Energy Source was manufactured in hours. The Factory Default operation shall not change the value of the ES_RUNTIME0 register. The ES_RUNTIME0 register is not impacted by the Factory Default operation.

5) ES_RUNTIME1 – Offset 0x74

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Total Energy Source runtime since manufacturing date MSB	RO	N	Y	0

The ES_RUNTIME1 register returns the most significant byte of the time the Energy Source has been operational since the Energy Source was manufactured in hours. The maximum value of this register is 255. Once this register has reach the maximum value, it shall stay at the maximum value. The ES_RUNTIME1 register is not impacted by the Factory Default operation.

B.2.3 Page 2 Register Map (Device Statistics, Error Injection, Host Area)

The registers in page 2 are related to device statistics, error injection or host area and organized based on categories. Table 8 shows the layout of the categories in page 2.

Table 136 - Page 2 categories

Offset	Category	Description
0x00 – 0x03	Paging Mechanism	Registers related to I ² C page support.
0x04 – 0x5F	Device Statistics	Registers providing device statistics information.
0x60 – 0x7F	Error Injection	Registers related to error injection support.
0x80 – 0xFF	Host Area	Registers for host generated data.

Table 9 shows the registers that are in page 2.

Table 137 - Page 2 register map

Offset	Register Name	Host Access Property	Mandatory	Persistent Across Power Cycles
0x00	OPEN_PAGE	RW	Y	N
0x01–0x03	Reserved			
0x04	LAST_SAVE_DURATION0	RO	N	Y
0x05	LAST_SAVE_DURATION1	RO	N	Y
0x06	Reserved	RO	N	Y
0x07	Reserved	RO	N	Y
0x08	LAST_ERASE_DURATION0	RO	N	Y
0x09	LAST_ERASE_DURATION1	RO	N	Y
0x0A	NUM_SAVE_OPS_COUNT0	RO	N	Y
0x0B	NUM_SAVE_OPS_COUNT1	RO	N	Y
0x0C	Reserved	RO	N	Y
0x0D	Reserved	RO	N	Y
0x0E	NUM_ERASE_OPS_COUNT0	RO	N	Y
0x0F	NUM_ERASE_OPS_COUNT1	RO	N	Y
0x10	NUM_MODULE_POWER_CYCLES0	RO	N	Y
0x11	NUM_MODULE_POWER_CYCLES1	RO	N	Y
0x12	NUM_SAVE_OPS_FAILURE_COUNT0	RO	N	Y
0x13	NUM_SAVE_OPS_FAILURE_COUNT1	RO	N	Y
0x14	Reserved	RO	N	Y
0x15	Reserved	RO	N	Y
0x16	NUM_ERASE_OPS_FAILURE_COUNT0	RO	N	Y
0x17	NUM_ERASE_OPS_FAILURE_COUNT1	RO	N	Y
0x18-0x5F	Reserved			
0x60	INJECT_OPS_FAILURES	RW	Y	Y
0x61	INJECT_OPS_FAILURES1	RW	Y	Y
0x62-0x63	Reserved			
0x64	INJECT_ES_FAILURES	RW	N	Y
0x65	INJECT_FW_FAILURES	RW	Y	Y
0x66	Reserved			
0x67	INJECT_BAD_BLOCK_CAP	RW	N	Y
0x68	INJECT_ERROR_TYPE	RW	N	Y
0x69-0x7F	Reserved			
0x80	NVM_ECC_ERROR_COUNT	RW	Y	Y
0x81	NVM_THRESHOLD_ECC_COUNT	RW	Y	Y
0x82	HOST_MANAGED_ES_ATTRIBUTES	RW	N	Y
0x83	HOST_CSAVE_FAIL	RW	Y	Y
0x84	HOST_CSAVE_WORKFLOW_FAILURE_COUNT0	RW	Y	Y
0x85	HOST_CSAVE_WORKFLOW_FAILURE_COUNT1	RW	Y	Y
0x86-0xFF	Reserved			

B.2.3.1 Paging Mechanism Registers

The registers in this section are related to the I²C paging mechanism supported by the module.

1) OPEN_PAGE – Offset 0x00

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Open page number	RW	Y	N	0

When the OPEN_PAGE register is read, it returns the current opened page number. When the OPEN_PAGE register is written to, the module shall attempt to set the current opened page number to the value written. The default value of OPEN_PAGE shall be 0.

B.2.3.2 Device Statistics Registers

The registers in this section provide device statistics information. If the module supports the register defined in this section, it shall set Bit 3 Device Statistics Supported in the CAPABILITIES register in page 0. If the module does not support these registers, the module shall return the value 0.

1) LAST_SAVE_DURATION0 – Offset 0x04

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Last Catastrophic Save duration LSB	RO	N	Y	0

The LAST_SAVE_DURATION0 register provides the least significant byte of the last Catastrophic Save duration in milliseconds or seconds.

2) LAST_SAVE_DURATION1 – Offset 0x05

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[6:0] : Last Catastrophic Save duration MSB [7] : 0 – Indicates duration in milliseconds 1 – Indicates duration in seconds	RO	N	Y	0

The LAST_SAVE_DURATION1 register provides the most significant byte of the last Catastrophic Save duration and the time unit for the Catastrophic Save duration.

If Bit 7 is 0, the Catastrophic Save duration value is in units of milliseconds. If Bit 7 is 1, the Catastrophic Save duration value is in units of seconds.

3) LAST_ERASE_DURATION0 – Offset 0x08

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Last Erase duration LSB	RO	N	Y	0

The LAST_ERASE_DURATION0 register provides the least significant byte of the last Erase duration in milliseconds or seconds.

4) LAST_ERASE_DURATION1 – Offset 0x09

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[6:0] : Last Erase duration MSB [7] : 0 – Indicates duration in milliseconds 1 – Indicates duration in seconds	RO	N	Y	0

The LAST_ERASE_DURATION1 register provides the most significant byte of the last Erase duration and the time unit for the Erase duration.

If Bit 7 is 0, the Erase duration value is in units of milliseconds. If Bit 7 is 1, the Erase duration value is in units of seconds.

5) NUM_SAVE_OPS_COUNT0 – Offset 0x0A

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of completed Catastrophic Save operations over the module lifetime LSB	RO	N	Y	0

The NUM_SAVE_OPS_COUNT0 provides the least significant byte of the number of completed Catastrophic Save operations over the module lifetime. The module shall increment the register value after the successful completion of a Catastrophic Save operation. The NUM_SAVE_OPS_COUNT0 register is not impacted by the Factory Default operation.

6) NUM_SAVE_OPS_COUNT1 – Offset 0x0B

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of completed Catastrophic Save operations over the module lifetime MSB	RO	N	Y	0

The NUM_SAVE_OPS_COUNT1 provides the most significant byte of the number of completed Catastrophic Save operations over the module lifetime. The module shall increment the register value after the successful completion of a Catastrophic Save operation. The maximum value of this register is 0xFF. When the register has reached its maximum value, the register shall stay at 0xFF. The NUM_SAVE_OPS_COUNT1 register is not impacted by the Factory Default operation.

Reserved for NUM_RESTORE_OPS_COUNT0 – Offset 0x0C

Reserved for NUM_RESTORE_OPS_COUNT1 – Offset 0x0D

7) NUM_ERASE_OPS_COUNT0 – Offset 0x0E

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of completed Erase operation over the module lifetime LSB	RO	N	Y	0

The NUM_ERASE_OPS_COUNT0 provides the least significant byte of the number of completed Erase operations over the module lifetime. Module shall increment the register value after the successful completion of an Erase operation.

8) NUM_ERASE_OPS_COUNT1 – Offset 0x0F

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of completed Erase operation over the module lifetime MSB	RO	N	Y	0

The NUM_ERASE_OPS_COUNT1 provides the most significant byte of the number of completed Erase operations over the module lifetime.

Module shall increment the register value after the successful completion of an Erase operation. The maximum value of this register is 255. When the register has reached its maximum value, the register shall stay at 255.

9) NUM_MODULE_POWER_CYCLES0 – Offset 0x10

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of power cycles over the module lifetime LSB	RO	N	Y	0

The NUM_MODULE_POWER_CYCLE0 provides the least significant byte of the number of power cycles over the module lifetime. Module shall increment the register value after the successful controller initialization. The NUM_MODULE_POWER_CYCLE0 register is not impacted by the Factory Default operation.

10) NUM_MODULE_POWER_CYCLES1 – Offset 0x11

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of power cycles over the module lifetime MSB	RO	N	Y	0

The NUM_MODULE_POWER_CYCLE1 provides the most significant byte of the number of power cycles over the module lifetime. Module shall increment the register value after the successful controller initialization. The maximum value of this register is 255. When the register has reached its maximum value, the register shall stay at 255. The NUM_MODULE_POWER_CYCLE1 register is not impacted by the Factory Default operation.

11) NUM_SAVE_OPS_FAILURE_COUNT0 – Offset 0x12

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of Catastrophic Save operation failures over the module lifetime LSB	RO	N	Y	0

The NUM_SAVE_OPS_FAILURE_COUNT0 provides the least significant byte of the number of Catastrophic Save failures over the module lifetime. Module shall increment the register value after each instance of a Catastrophic Save failure.

12) NUM_SAVE_OPS_FAILURE_COUNT1 – Offset 0x13

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of Catastrophic Save operation failures over the module lifetime MSB	RO	N	Y	0

The NUM_SAVE_OPS_FAILURE_COUNT1 provides the most significant byte of the number of Catastrophic Save failures over the module lifetime. Module shall increment the register value after each instance of a Catastrophic Save failure.

The maximum value of this register is 255. When the register has reached its maximum value, the register shall stay at 255. The NUM_SAVE_OPS_FAILURE_COUNT1 register is not impacted by the Factory Default operation.

Reserved for NUM_RESTORE_OPS_FAILURE_COUNT0 – Offset 0x14

Reserved for NUM_RESTORE_OPS_FAILURE_COUNT1 – Offset 0x15

13) NUM_ERASE_OPS_FAILURE_COUNT0 – Offset 0x16

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of Erase operation failures over the module lifetime LSB	RO	N	Y	0

The NUM_ERASE_OPS_FAILURE_COUNT0 provides the least significant byte of the number of Erase failures over the module lifetime. Module shall increment the register value after each instance of an Erase failure.

14) NUM_ERASE_OPS_FAILURE_COUNT1 – Offset 0x17

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of Erase operation failures over the module lifetime MSB	RO	N	Y	0

The NUM_ERASE_FAILURE_COUNT1 provides the most significant byte of the number of Erase failures over the module lifetime. Module shall increment the register value after each instance of an Erase failure.

The maximum value of this register is 255. When the register has reached its maximum value, the register shall stay at 255. The NUM_ERASE_OPS_FAILURE_COUNT1 register is not impacted by the Factory Default operation.

B.2.3.3 Error Injection Registers

The registers in this section are related to error injection support.

1) INJECT_OPS_FAILURES – Offset 0x60

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : INJECT_SAVE_FAILURE [1] : Reserved [2] : INJECT_ERASE_FAILURE [3] : Reserved [4] : INJECT_INTERNAL_CONTROLLER_FAILURE [5] : INJECT_NVM_LIFETIME_WARNING [6] : INJECT_NVM_LIFETIME_ERROR [7] : INJECT_BAD_BLOCKS	RW	Y	Y	0

The INJECT_OPS_FAILURES register allows a Host to inject operation or non-volatile memory related failures. A set bit indicates the corresponding error injection is enabled. A clear bit indicates the corresponding error injection is disabled. Error injection shall take place on the next applicable operation. If Bit 0 of INJECT_ERROR_TYPE (page 2 offset 0x68) is not set, the error injection is enabled until explicitly disabled. One or more bits can be set in this register.

If Bit 0, INJECT_SAVE_FAILURE, is set, module shall cause the next Catastrophic Save operation that is initiated to fail. The failure to inject is implementation specific.

If Bit 1, Reserved.

If Bit 2, INJECT_ERASE_FAILURE, is set, module shall cause the next Erase operation to fail after Erase operation has been initiated. The failure to inject is implementation specific.

If Bit 3, Reserved.

If Bit 4, INJECT_INTERNAL_CONTROLLER_FAILURE, is set, module shall inject an internal controller failure at the most appropriate time.

If Bit 5, INJECT_NVM_LIFETIME_WARNING, is set, module shall simulate a NVM lifetime warning threshold exceeded event.

If Bit 6, INJECT_NVM_LIFETIME_ERROR, is set, module shall simulate a NVM lifetime error threshold exceeded event.

If Bit 7, INJECT_BAD_BLOCKS, is set, module shall disable bad block correction until the percentage of NVM that contains a bad block matches INJECT_BAD_BLOCK_CAP register value. This support is optional.

2) INJECT_OPS_FAILURES1 – Offset 0x61

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : INJECT_PERMANENT_HARDWARE_FAILURE [7:1] : Reserved	RW	Y	Y	0

The INJECT_OPS_FAILURES1 register allows a Host to inject failures. A set bit indicates the corresponding error injection is enabled. A clear bit indicates the corresponding error injection is disabled. Error injection shall take place on the next applicable operation. If Bit 0 of INJECT_ERROR_TYPE (page 2 offset 0x68) is not set, the error injection is enabled until explicitly disabled. One or more bits can be set in this register.

If Bit 0, INJECT_PERMANENT_HARDWARE_FAILURE, is set, module shall cause the module to report that it has a permanent hardware failure.

3) INJECT_ES_FAILURES – Offset 0x64

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : INJECT_ES_FAILURE [1] : INJECT_ES_ASSESSMENT_FAILURE [2] : INJECT_ES_LIFETIME_WARNING [3] : INJECT_ES_LIFETIME_ERROR [4] : INJECT_ES_TEMP_WARNING [5] : INJECT_ES_TEMP_ERROR [7:6] : Reserved	RW	N	Y	0

The INJECT_ES_FAILURES register allows a Host to inject errors into Device managed Energy Source. A set bit indicates the corresponding error injection is enabled. A clear bit indicates the corresponding error injection is disabled. Error injection shall take place on the next applicable operation. If Bit 0 of INJECT_ERROR_TYPE (page 2 offset 0x68) is not set, the error injection is enabled until explicitly disabled. One or more bits can be set in this register.

This register shall be supported when module is in Device Managed Policy mode. When the module is in Host Managed Policy mode, module shall return the value 0 if this register is read and ignore writes to this register.

If Bit 0, INJECT_ES_FAILURE, is set, module shall simulate an Energy Source hardware failure.

If Bit 1, INJECT_ES_ASSESSMENT_FAILURE, is set, module shall fail the next Energy Source health check.

If Bit 2, INJECT_ES_LIFETIME_WARNING, is set, module shall simulate an Energy Source lifetime warning threshold exceeded event.

If Bit 3, INJECT_ES_LIFETIME_ERROR, is set, module shall simulate an Energy Source lifetime error threshold exceeded event.

If Bit 4, INJECT_ES_TEMP_WARNING, is set, module shall simulate an Energy Source temperature warning threshold exceeded event.

If Bit 5, INJECT_ES_TEMP_ERROR, is set, module shall simulate an Energy Source temperature error threshold exceeded event.

4) INJECT_FW_FAILURES – Offset 0x65

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : INJECT_FW_COMMIT_FAILURE [1] : INJECT_FW_CHECKSUM_FAILURE [2] : INJECT_INVALID_FW [7:3] : Reserved	RW	Y	Y	0

The INJECT_FW_FAILURES register allows a Host to inject errors for firmware related operations. A set bit indicates the corresponding error injection is enabled. A clear bit indicates the corresponding error injection is disabled. Error injection shall take place on the next applicable operation. If Bit 0 of INJECT_ERROR_TYPE (page 2 offset 0x68) is not set, the error injection is enabled until explicitly disabled. One or more bits can be set in this register.

If Bit 0, INJECT_FW_COMMIT_FAILURE, is set, module shall fail the next commit firmware data region operation.

If Bit 1, INJECT_FW_CHECKSUM_FAILURE, is set, module shall inject a bad checksum value to FW_REGION_CRC0 and FW_REGION_CRC1 registers for the next generate firmware data region checksum operation.

If Bit 2, INJECT_INVALID_FW, is set, module shall fail the next validate firmware image operation. If this bit is set during controller initialization, module shall treat the firmware in slot 1 as an invalid firmware image.

5) INJECT_BAD_BLOCK_CAP – Offset 0x67

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Maximum percentage of NVM containing bad block	RW	N	Y	0

The INJECT_BAD_BLOCK_CAP register allows a Host to set the maximum percentage of non-volatile memory that contains a bad block when INJECT_BAD_BLOCKS error injection is enabled. Host shall set this register to a non-zero value prior to enabling INJECT_BAD_BLOCKS.

6) INJECT_ERROR_TYPE – Offset 0x68

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : ONE_TIME_USE [7:1] Reserved	RW	N	Y	0

The INJECT_ERROR_TYPE register allows a Host to set whether the error injection is one-time only or persistent until disabled.

If Bit 0, ONE_TIME_USE, is 0, the error injection is persistent until disabled. If Bit 0 is 1, the error injection is one-time only.

B.2.3.4 Host Area Registers

The registers in this section are related to Host generated data. Modules shall only provide storage for these data and do not act upon the data.

1) NVM_ECC_ERROR_COUNT – Offset 0x80

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of uncorrectable ECC errors detected on the module	RW	Y	Y	0

The NVM_ECC_ERROR_COUNT register contains the number of uncorrectable ECC errors detected by the Host from the module. Host should increment this register every time it detects an uncorrectable ECC from the module. The maximum value of this register is 255. Once the register reaches the value 255, it shall stay at 255.

2) NVM_THRESHOLD_ECC_COUNT – Offset 0x81

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of correctable ECC threshold exceeded events detected on the module	RW	Y	Y	0

The NVM_THRESHOLD_ECC_COUNT register contains the number of correctable ECC threshold exceeded events detected by the Host from the module. Host should increment this register every time it detects a correctable ECC error has exceeded the configured correctable ECC threshold for the module. The maximum value of this register is 255. Once the register reaches the value 255, it shall stay at 255.

3) HOST_MANAGED_ES_ATTRIBUTES – Offset 0x82

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : Shared - 0: Dedicated Energy Source - 1: Shared Energy Source [7:1] Reserved	RW	N	Y	0

The HOST_MANAGED_ES_ATTRIBUTES register allows a Host to store attributes for the Host managed Energy Source that moves with the module. A module in Host Managed Policy mode shall support this register. A module in Device Managed Policy mode shall return the value 0 if this is register is read and ignore any writes to this register.

If Bit 0 is set to 0, the Host managed Energy Source is used only by this module. If Bit 0 is set to 1, the Host managed Energy Source is shared by two or more modules.

4) HOST_CSAVE_FAIL – Offset 0x83

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[0] : HOST_ES_FAIL [1] : MC_WRITE_BUFFER_FLUSH_FAIL [2] : CPU_CACHE_FLUSH_FAIL [3] : IO_DMA_WRITE_BUFFER_FLUSH_FAIL [4] : HOST_CSAVE_WORKFLOW_FAIL [7:5] Reserved	RW	Y	Y	0

The HOST_CSAVE_FAIL register allows a Host to store information about issues on the Host that causes a Catastrophic Save operation to fail or inconsistent data to be saved during a Catastrophic Save operation.

If Bit 0, HOST_ES_FAIL is set, the Catastrophic Save operation failed due to a Host Energy Source issue.

If Bit 1, MC_WRITE_BUFFER_FLUSH_FAIL, is set, the Host encounters a failure flushing the media controller's write buffer(s).

If Bit 2, CPU_CACHE_FLUSH_FAIL, is set, the Host encounter a failure flushing the processor cache(s).

If Bit 3, IO_DMA_WRITE_BUFFER_FLUSH_FAIL, is set, the Host encounter a failure flushing the write buffer used for IO DMA.

If Bit 4, HOST_CSAVE_WORKFLOW_FAIL, is set, the Host encounter a non-cache or write buffer flush failure in its Catastrophic Save workflow.

5) HOST_CSAVE_WORKFLOW_FAILURE_COUNT0 – Offset 0x84

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of Host Catastrophic Save Workflow failures LSB	RO	N	Y	0

The HOST_CSAVE_WORKFLOW_FAILURE_COUNT0 provides the least significant byte of the number of Host Catastrophic Save Workflow failures. Host Catastrophic Save Workflow failures includes all failures on the host that cause a Catastrophic Save to fail or inconsistent data to be saved.

6) HOST_CSAVE_WORKFLOW_FAILURE_COUNT1 – Offset 0x85

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Number of Host Catastrophic Save Workflow failures MSB	RO	N	Y	0

The HOST_CSAVE_WORKFLOW_FAILURE_COUNT0 provides the most significant byte of the number of Host Catastrophic Save Workflow failures. Host Catastrophic Save Workflow failures includes all failures on the host that cause a Catastrophic Save to fail or inconsistent data to be saved.

The maximum value of this register is 255. When the register has reached its maximum value, the register shall stay at 255.

B.2.4 Page 3 Register Map (Typed Block Data, Firmware Update)

The registers in page 3 are related to Typed Block Data support or firmware update and organized based on categories. Table 10 shows the layout of the categories in page 3.

Table 138 - Page 3 categories

Offset	Category	Description
0x00 – 0x03	Paging Mechanism	Registers related to I ² C page support.
0x04 – 0x3F	Typed Block Data	Registers related to Typed Block Data support.
0x40 – 0x6F	Firmware Update	Registers related to firmware update support.
0x70 – 0x7F	Reserved	Reserved
0x80 – 0xBF	Typed Block Data Byte Data	Registers for Typed Block Data byte transfer.
0xC0 – 0xDF	Reserved	Reserved
0xE0 – 0xFF	Typed Block Data Block Data	Registers for Typed Block Data block transfer.

Table 11 shows the registers that are in page 3.

Table 139 - Page 3 register map

Offset	Register Name	Host Access Property	Mandatory	Persistent Across Power Cycles
0x00	OPEN_PAGE	RW	Y	N
0x01–0x03	Reserved			
0x04	TYPED_BLOCK_DATA	RW	Y	N
0x05	REGION_ID0	RW	Y	N
0x06	REGION_ID1	RW	Y	N
0x07	BLOCK_ID	RW	Y	N
0x08	TYPED_BLOCK_DATA_SIZE0	RO	Y	N
0x09	TYPED_BLOCK_DATA_SIZE1	RO	Y	N
0x0A	TYPED_BLOCK_DATA_SIZE2	RO	Y	N
0x0B	Reserved			
0x0C	OPERATIONAL_UNIT_ID0	WO	Y	N
0x0D	OPERATIONAL_UNIT_ID1	WO	Y	N
0x0E–0x0F	Reserved			
0x10	OPERATIONAL_UNIT_SIZE0	RO	Y	N
0x11	OPERATIONAL_UNIT_SIZE1	RO	Y	N
0x12	OPERATIONAL_UNIT_SIZE2	RO	Y	N

0x13	Reserved			
0x14	OPERATIONAL_UNIT_CRC0	RO	Y	N
0x15	OPERATIONAL_UNIT_CRC1	RO	Y	N
0x16-0x3F	Reserved			
0x40	FW_REGION_CRC0	RO	Y	N
0x41	FW_REGION_CRC1	RO	Y	N
0x42	FW_SLOT_INFO	RW	Y	Y
0x43-0x7F	Reserved			
0x80	TYPED_BLOCK_DATA_BYTE0	RW	Y	N
0x81	TYPED_BLOCK_DATA_BYTE1	RW	Y	N
0x82	TYPED_BLOCK_DATA_BYTE2	RW	Y	N
0x83	TYPED_BLOCK_DATA_BYTE3	RW	Y	N
0x84	TYPED_BLOCK_DATA_BYTE4	RW	Y	N
0x85	TYPED_BLOCK_DATA_BYTE5	RW	Y	N
0x86	TYPED_BLOCK_DATA_BYTE6	RW	Y	N
0x87	TYPED_BLOCK_DATA_BYTE7	RW	Y	N
0x88	TYPED_BLOCK_DATA_BYTE8	RW	Y	N
0x89	TYPED_BLOCK_DATA_BYTE9	RW	Y	N
0x8A	TYPED_BLOCK_DATA_BYTE10	RW	Y	N
0x8B	TYPED_BLOCK_DATA_BYTE11	RW	Y	N
0x8C	TYPED_BLOCK_DATA_BYTE12	RW	Y	N
0x8D	TYPED_BLOCK_DATA_BYTE13	RW	Y	N
0x8E	TYPED_BLOCK_DATA_BYTE14	RW	Y	N
0x8F	TYPED_BLOCK_DATA_BYTE15	RW	Y	N
0x90	TYPED_BLOCK_DATA_BYTE16	RW	Y	N
0x91	TYPED_BLOCK_	RW	Y	N

	DATA_BYTE17			
0x92	TYPED_BLOCK_ DATA_BYTE18	RW	Y	N
0x93	TYPED_BLOCK_ DATA_BYTE19	RW	Y	N
0x94	TYPED_BLOCK_ DATA_BYTE20	RW	Y	N
0x95	TYPED_BLOCK_ DATA_BYTE21	RW	Y	N
0x96	TYPED_BLOCK_ DATA_BYTE22	RW	Y	N
0x97	TYPED_BLOCK_ DATA_BYTE23	RW	Y	N
0x98	TYPED_BLOCK_ DATA_BYTE24	RW	Y	N
0x99	TYPED_BLOCK_ DATA_BYTE25	RW	Y	N
0x9A	TYPED_BLOCK_ DATA_BYTE26	RW	Y	N
0x9B	TYPED_BLOCK_ DATA_BYTE27	RW	Y	N
0x9C	TYPED_BLOCK_ DATA_BYTE28	RW	Y	N
0x9D	TYPED_BLOCK_ DATA_BYTE29	RW	Y	N
0x9E	TYPED_BLOCK_ DATA_BYTE30	RW	Y	N
0x9F	TYPED_BLOCK_ DATA_BYTE31	RW	Y	N
0xA0 – 0xDF	Reserved			
0xE0	TYPED_BLOCK_ DATA_OFFSET	RW	N	N
0xE1-0xFF	Reserved			

B.2.4.1 Paging Mechanism Registers

The registers in this section are related to the I²C paging mechanism supported by the module.

1) OPEN_PAGE – Offset 0x00

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] Open page number	RW	Y	N	0

When the OPEN_PAGE register is read, it returns the current opened page number. When the OPEN_PAGE register is written to, the module shall attempt to set the current opened page number to the value written. The default value of OPEN_PAGE shall be 0.

B.2.4.2 Typed Block Data Registers

The registers in this section are related to the Typed Block Data feature supported by the module.

1) TYPED_BLOCK_DATA – Offset 0x04

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : TYPED_BLOCK_DATA - 0: Reserved - 1: Firmware image data - 2: Vendor Log Page - 3: Label Data - 4 to 200: Reserved - 201 to 255: Vendor Specific	RW	Y	N	0

When read from, the TYPED_BLOCK_DATA register provides the last Typed Block Data type that was written by the Host. When written to, the TYPED_BLOCK_DATA register sets the Typed Block Data type of subsequent read or write to Typed Block Data register offsets. Hosts shall set TYPED_BLOCK_DATA register with the appropriate TYPED_BLOCK_DATA type value before transferring any Typed Block Data bytes.

If the TYPED_BLOCK_DATA is set to 1, the DATA_BLOB type is firmware image data.

If the TYPED_BLOCK_DATA is set to 2, the DATA_BLOB type is Vendor Log Page.

If the TYPED_BLOCK_DATA is set to 3, the DATA_BLOCK type is Label Data.

TYPED_BLOCK_DATA values from 201 to 255 are reserved for vendor specific usage.

2) REGION_ID0 – Offset 0x05

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : REGION_ID LSB	RW	Y	N	0

When read from, the REGION_ID0 register provides the least significant byte of the region identifier. When written to, the Host sets the least significant byte of the region identifier of subsequent Typed Block Data transfers.

Hosts use the REGION_ID0 and REGION_ID1 registers to communicate to the module the region identifier of subsequent Typed Block Data transfers. The first region identifier has a value of 0.

3) REGION_ID1 – Offset 0x06

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : REGION_ID MSB	RW	Y	N	0

When read from, the REGION_ID1 register provides the most significant byte of the region identifier. When written to, the Host sets the most significant byte of the region identifier of subsequent Typed Block Data transfers.

Hosts use the REGION_ID0 and REGION_ID1 registers to communicate to the module the region identifier of subsequent Typed Block Data transfers. The first region identifier has a value of 0.

4) BLOCK_ID – Offset 0x07

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : BLOCK_ID	RW	Y	N	0

When read from, the BLOCK_ID register provides the block identifier that was last written. When written to, the Host sets the block identifier of subsequent Typed Block Data transfers.

The first block identifier has a value of 0.

5) TYPED_BLOCK_DATA_SIZE0 – Offset 0x08

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : TYPED_BLOCK_DATA_SIZE Byte 0 (LSB)	RO	Y	N	0

The TYPED_BLOCK_DATA_SIZE0 contains the least significant byte of the size of the current TYPED_BLOCK_DATA type. The Typed Block Data Size is in 32 bytes multiple. A reserved TYPED_BLOCK_DATA type shall return a Typed Block Data Size of 0.

6) TYPED_BLOCK_DATA_SIZE1 – Offset 0x09

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : TYPED_BLOCK_DATA_SIZE Byte 1	RO	Y	N	0

The TYPED_BLOCK_DATA_SIZE0 contains the second least significant byte of the size of the current TYPED_BLOCK_DATA type. The Typed Block Data Size is in 32 bytes multiple. A reserved TYPED_BLOCK_DATA type shall return a Typed Block Data Size of 0.

7) TYPED_BLOCK_DATA_SIZE2 – Offset 0x0A

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : TYPED_BLOCK_DATA_SIZE Byte 2 (MSB)	RO	Y	N	0

The TYPED_BLOCK_DATA_SIZE0 contains the most significant byte of the size of the current TYPED_BLOCK_DATA type. The Typed Block Data Size is in 32 bytes multiple. A reserved TYPED_BLOCK_DATA type shall return a Typed Block Data Size of 0.

8) OPERATIONAL_UNIT_ID0 – Offset 0x0C

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : OPERATIONAL_UNIT_ID LSB	WO	Y	N	0

The OPERATIONAL_UNIT_ID0 contains the least significant byte of the Operational Unit ID that will be used for subsequent Typed Data Block transfers. This is a write only register that the host sets before doing any Typed Block Data transfers to a TYPED_BLOCK_DATA type.

9) OPERATIONAL_UNIT_ID1 – Offset 0x0D

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : OPERATIONAL_UNIT_ID MSB	WO	Y	N	0

The OPERATIONAL_UNIT_ID1 contains the most significant byte of the Operational Unit ID that will be used for subsequent Typed Data Block transfers. This is a write only register that the host sets before doing any Typed Block Data transfers to a TYPED_BLOCK_DATA type.

10) OPERATIONAL_UNIT_SIZE0 – Offset 0x10

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : OPERATIONAL_UNIT_SIZE Byte 0 (LSB)	RO	Y	N	0

The OPERATIONAL_UNIT_SIZE0 contains the least significant byte of the Operational Unit size for the current TYPED_BLOCK_DATA type. The Operational Unit size is in units of 32 bytes. A reserved TYPED_BLOCK_DATA type shall return an Operational Unit size of 0.

11) OPERATIONAL_UNIT_SIZE1 – Offset 0x11

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : OPERATIONAL_UNIT_SIZE Byte 1	RO	Y	N	0

The OPERATIONAL_UNIT_SIZE1 contains the second least significant byte of the Operational Unit size for the current TYPED_BLOCK_DATA type. The Operational Unit size is in units of 32 bytes. A reserved TYPED_BLOCK_DATA type shall return an Operational Unit size of 0.

12) OPERATIONAL_UNIT_SIZE2 – Offset 0x12

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : OPERATIONAL_UNIT_SIZE Byte 2 (MSB)	RO	Y	N	0

The OPERATIONAL_UNIT_SIZE2 contains the most significant byte of the Operational Unit size for the current TYPED_BLOCK_DATA type. The Operational Unit size is in units of 32 bytes. A reserved TYPED_BLOCK_DATA type shall return an Operational Unit size of 0.

13) OPERATIONAL_UNIT_CRC0 – Offset 0x14

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : OPERATIONAL_UNIT_CRC LSB	RO	Y	N	0

The OPERATIONAL_UNIT_CRC0 contains the least significant byte of the CRC that is generated by the Generate Operational Unit Checksum operation. If a CRC has not been generated for the current Operational Unit, the module shall return a value of 0.

14) OPERATIONAL_UNIT_CRC1 – Offset 0x15

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : OPERATIONAL_UNIT_CRC MSB	RO	Y	N	0

The OPERATIONAL_UNIT_CRC1 contains the most significant byte of the CRC that is generated by the Generate Operational Unit Checksum operation. If a CRC has not been generated for the current Operational Unit, the module shall return a value of 0.

B.2.4.3 Firmware Update Registers

The registers in this section are related to firmware update.

1) FW_REGION_CRC0 – Offset 0x40

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Calculated checksum for firmware data region LSB	RO	Y	N	0

The FW_REGION_CRC0 register provides the least significant byte of the calculated checksum for the firmware data region.

Hosts shall read the FW_REGION_CRC0 and FW_REGION_CRC1 registers after transfer of each firmware data region to confirm data was transferred correctly between the Host and module.

2) FW_REGION_CRC1 – Offset 0x41

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Calculated checksum for firmware data region MSB	RO	Y	N	0

The FW_REGION_CRC1 register provides the most significant byte of the calculated checksum for the firmware data region.

Hosts shall read the FW_REGION_CRC0 and FW_REGION_CRC1 registers after transfer of each firmware data region to confirm data was transferred correctly between the Host and module.

3) FW_SLOT_INFO – Offset 0x42

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[3:0] : SELECT_FW_SLOT – Host selected firmware slot	RW	Y	Y	0
[7:4] : RUNNING_FW_SLOT – slot number of running firmware.				

The FW_SLOT_INFO register provides information on the slot number of the running firmware image and the slot number of intended firmware image. The values of SELECT_FW_SLOT and RUNNING_FW_SLOT shall be either 0 or 1. All other values are reserved. The FW_SLOT_INFO register is not impacted by the Factory Default operation.

If SELECT_FW_SLOT is set to 1 and firmware slot 1 is empty or contains an invalid firmware image, the value of RUNNING_FW_SLOT shall be 0.

B.2.4.4 Typed Block Data Byte Data Registers

The registers in this section support transferring Typed Block Data bytes using I²C byte operations.

1) TYPED_BLOCK_DATA_BYTE0 – Offset 0x80

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 0	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE0 register contains byte 0 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

2) TYPED_BLOCK_DATA_BYTE1 – Offset 0x81

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 1	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE1 register contains byte 1 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

3) TYPED_BLOCK_DATA_BYTE2 – Offset 0x82

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 2	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE2 register contains byte 2 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

4) TYPED_BLOCK_DATA_BYTE3 – Offset 0x83

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 3	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE3 register contains byte 3 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

5) TYPED_BLOCK_DATA_BYTE4 – Offset 0x84

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 4	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE4 register contains byte 4 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

6) TYPED_BLOCK_DATA_BYTE5 – Offset 0x85

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 5	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE5 register contains byte 5 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

7) TYPED_BLOCK_DATA_BYTE6 – Offset 0x86

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 6	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE6 register contains byte 6 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

8) TYPED_BLOCK_DATA_BYTE7 – Offset 0x87

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 7	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE7 register contains byte 7 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

9) TYPED_BLOCK_DATA_BYTE8 – Offset 0x88

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 8	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE8 register contains byte 8 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

10) TYPED_BLOCK_DATA_BYTE9 – Offset 0x89

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 9	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE9 register contains byte 9 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

11) TYPED_BLOCK_DATA_BYTE10 – Offset 0x8A

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 10	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE10 register contains byte 10 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

12) TYPED_BLOCK_DATA_BYTE11 – Offset 0x8B

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 11	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE11 register contains byte 11 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

13) TYPED_BLOCK_DATA_BYTE12 – Offset 0x8C

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 12	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE12 register contains byte 12 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

14) TYPED_BLOCK_DATA_BYTE13 – Offset 0x8D

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 13	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE13 register contains byte 13 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

15) TYPED_BLOCK_DATA_BYTE14 – Offset 0x8E

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 14	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE14 register contains byte 14 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

16) TYPED_BLOCK_DATA_BYTE15 – Offset 0x8F

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 15	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE15 register contains byte 15 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

17) TYPED_BLOCK_DATA_BYTE16 – Offset 0x90

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 16	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE16 register contains byte 16 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

18) TYPED_BLOCK_DATA_BYTE17 – Offset 0x91

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 17	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE17 register contains byte 17 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

19) TYPED_BLOCK_DATA_BYTE18 – Offset 0x92

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 18	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE18 register contains byte 18 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

20) TYPED_BLOCK_DATA_BYTE19 – Offset 0x93

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 19	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE19 register contains byte 19 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

21) TYPED_BLOCK_DATA_BYTE20 – Offset 0x94

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 20	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE20 register contains byte 20 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

22) TYPED_BLOCK_DATA_BYTE21 – Offset 0x95

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 21	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE21 register contains byte 21 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

23) TYPED_BLOCK_DATA_BYTE22 – Offset 0x96

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 22	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE22 register contains byte 22 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

24) TYPED_BLOCK_DATA_BYTE23 – Offset 0x97

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 23	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE23 register contains byte 23 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

25) TYPED_BLOCK_DATA_BYTE24 – Offset 0x98

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 24	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE24 register contains byte 24 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

26) TYPED_BLOCK_DATA_BYTE25 – Offset 0x99

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 25	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE25 register contains byte 25 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

27) TYPED_BLOCK_DATA_BYTE26 – Offset 0x9A

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 6	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE26 register contains byte 26 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

28) TYPED_BLOCK_DATA_BYTE27 – Offset 0x9B

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 27	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE27 register contains byte 27 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

29) TYPED_BLOCK_DATA_BYTE28 – Offset 0x9C

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 28	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE28 register contains byte 28 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

30) TYPED_BLOCK_DATA_BYTE29 – Offset 0x9D

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 29	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE29 register contains byte 29 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

31) TYPED_BLOCK_DATA_BYTE30 – Offset 0x9E

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 30	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE30 register contains byte 30 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

32) TYPED_BLOCK_DATA_BYTE31 – Offset 0x9F

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : Typed Block Data Byte 31	RW	Y	N	0

The TYPED_BLOCK_DATA_BYTE31 register contains byte 31 of the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

B.2.4.5 Typed Block Data Block Data Registers

The registers in this section support transferring Typed Block Data bytes using I²C block operations.

1) TYPED_BLOCK_DATA_OFFSET – Offset 0xE0

Definition	Host Access Property	Mandatory	Persistent Across Power Cycle	Default
[7:0] : TYPED_BLOCK_DATA_OFFSET	RW	N	N	0

The TYPED_BLOCK_DATA_OFFSET register is the offset used to transfer a block of Typed Block Data bytes using I²C block read or block write commands. The data transferred is for the block with identifier BLOCK_ID and region identifier REGION_ID0 and REGION_ID1.

B.3 Host Operation Workflows

This section describes the workflow for various operations from the Host perspective.

B.3.1 Controller Ready Workflow

To determine whether the module is ready for host access on system boot or after a controller reset, the Host shall do the following:

1. Read offset 0x60 in page 0 until the value read is equal to 0xA5 or timeout occurs. The timeout is reported in SPD byte 203 Maximum Non-Volatile Memory Initialization Time.

Prior to the controller being ready, the Host shall only access I²C registers at offsets 0x0, 0x60, 0xA0 and 0xA1 in page 0.

B.3.2 Catastrophic Save Workflow

To initiate a Catastrophic Save operation through the I²C register, the Host shall do the following:

1. Read NVDIMM_CMD_STATUS0 register and wait for bit 0 to be clear (Controller NOT busy).
2. Write 0x4 (CL_SAVE_SET) to the NVDIMM_MGT_CMD0 register to clear save status register.
3. NVDIMM_FUNC_CMD0: START_SAVE
4. NVDIMM_CMD_STATUS0: check for SAVE in progress bit to be set. If not set, check for SAVE to be done in SAVE_STATUS0. If save not done, retry step 3.
5. NVDIMM_CMD_STATUS0: wait for SAVE in progress bit to be clear. If SAVE in progress bit is not clear after CSAVE_TIMEOUT, abort the SAVE (see Section B.3.4).
6. SAVE_STATUS0: check for either SAVE successful or error. If error or save aborted, Host may retry up to the Maximum Catastrophic Save retry count indicated in HOST_MAX_OPERATION_RETRY.

B.3.3 Erase Workflow

To initiate an erase, the Host shall do the following:

1. NVDIMM_CMD_STATUS0: wait for Controller NOT busy.
2. NVDIMM_MGT_CMD0: set CL_ERASE_STAT to clear restore status register.
3. NVDIMM_FUNC_CMD0: START_ERASE
4. NVDIMM_CMD_STATUS0: check for ERASE in progress bit to be set. If not set, check for ERASE to be done in ERASE_STATUS0. If erase not done, retry step 3.
5. NVDIMM_CMD_STATUS0: wait for ERASE in progress bit to be clear. If the ERASE in progress bit is not clear after ERASE_TIMEOUT, abort the ERASE (see B.3.4).
6. ERASE_STATUS0: check for either ERASE successful or error. If error or ERASE aborted, Host may retry up to the Maximum Erase retry count indicated in HOST_MAX_OPERATION_RETRY.

B.3.4 Abort Running Operation Workflow

To abort the current running operation, the Host shall do the following:

1. NVDIMM_FUNC_CMD0: ABORT_CURRENT_OP
2. NVDIMM_CMD_STATUS0: check for ABORT in progress bit to be set. If not set, check for ABORT to be done. If abort not done, retry step 1.
3. NVDIMM_CMD_STATUS0: wait for ABORT in progress bit to be clear. When clear, the running operation in progress bit shall also be clear. Max wait ABORT_CMD_TIMEOUT.
4. Running operation status register: check for either ABORT successful or failure.

B.3.5 Firmware Update Workflow

Firmware image data is transferred and committed to the module in `REGION_BLOCK_SIZE` size. To update a firmware image on the module, the Host should do the following:

1. Validates that the Module Manufacturer ID and Module Product Identifier in the common header of the firmware image matches the values stored in the module's SPD (bytes 320 and 321 for the Module Manufacturer ID and bytes 192 and 193 for the Module Product Identifier) If the values do not match, abort the firmware update and do not transfer any data to the module. Host may do additional verification by verifying the calculated checksum of the image data matches the checksum in the common header.
2. Validates controller is not busy.
 - a. Reads `NVDIMM_CMD_STATUS0` register and waits for controller not busy (bit 0 to 0).
3. Clears the firmware ops status register.
 - a. Writes `NVDIMM_MGT_CMD1` register with value 0x2 (`CL_FIRMWARE_OPS_STAT` to 1).
4. Enable firmware update mode.
 - a. Writes `FIRMWARE_OPS_CMD` register with the value 0x1 to enable firmware update mode.
 - b. Check for `FIRMWARE_OPS` in progress bit (bit 7) to be set in `NVDIMM_CMD_STATUS0` register.
 - c. If `FIRMWARE_OPS` in progress bit is set, wait for `FIRMWARE_OPS` in progress bit to be clear for a maximum of `FIRMWARE_OPS_TIMEOUT`. If `FIRMWARE_OPS` in progress bit is not clear after `FIRMWARE_OPS_TIMEOUT`, abort the `FIRMWARE_OPS` command and abort firmware update.
 - d. If `FIRMWARE_OPS` in progress bit is not set, check `FIRMWARE_OPS_STATUS` register for status of enable firmware update mode. If not successful, abort the firmware update.
 - e. In firmware update mode, no other operations are supported.
 - f. Verify firmware update mode bit (bit 2) it set to 1 in `FIRMWARE_OPS_STATUS` register.
5. Clears the firmware ops status register.
 - a. Writes `NVDIMM_MGT_CMD1` register with value 0x2 (`CL_FIRMWARE_OPS_STAT` to 1).
6. Clears the firmware data block to ensure there is no residual data.
 - a. Writes `FIRMWARE_OPS_CMD` register with value 0x2 (clear firmware data block).
 - b. Check for `FIRMWARE_OPS` in progress bit to be set in `NVDIMM_CMD_STATUS0` register.
 - c. If `FIRMWARE_OPS` in progress bit is set, wait for `FIRMWARE_OPS` in progress bit to be clear for a maximum of `FIRMWARE_OPS_TIMEOUT`. If `FIRMWARE_OPS` in progress bit is not clear after `FIRMWARE_OPS_TIMEOUT`, abort the `FIRMWARE_OPS` command and abort firmware update.
 - d. If `FIRMWARE_OPS` in progress bit is not set, check `FIRMWARE_OPS_STATUS` register for status of clear firmware data block. If not successful, abort the firmware update.
7. Sends the data for the first firmware data region.
 - a. Writes `TYPED_BLOCK_DATA` register with value 0x1 (firmware image data).
 - b. Writes `BLOCK_ID`, `REGION_ID0` and `REGION_ID1` registers with value 0.
 - c. Send the bytes from the first firmware data region to the module using either I²C block write to the `TYPED_BLOCK_DATA_OFFSET` register or I²C write byte to the `TYPED_BLOCK_DATA_BYTES0` to `TYPED_BLOCK_DATA_BYTES31`. Data transfer will be done in 32 byte multiple. After a block has been transferred, verify that the 32-byte `BLOCK` is received by polling `FIRMWARE_OPS_STATUS` offset for `FIRMWARE_BLOCK_RECEIVED`. Once the block is successfully received by the NVDIMM, increment and write the updated block identifier to the `BLOCK_ID` register and keep transferring blocks of data until all data in the region has been sent.

- d. Host validates that the data was transferred correctly to the module by ensuring checksum calculated by module matches the Host for the firmware data region that has been transferred.
 - i. Calculates the checksum for the firmware data region transferred using the checksum algorithm described Section B.1.15.1.
 - ii. Clear the firmware ops status register. Write NVDIMM_MGT_CMD1 register with value 0x2 (CL_FIRMWARE_OPS_STAT to 1).
 - iii. Commands the module to calculate checksum for the firmware data region. Write FIRMWARE_OPS_CMD register with value 0x4 (generate firmware data region checksum).
 - iv. Check for FIRMWARE_OPS in progress bit to be set in NVDIMM_CMD_STATUS0 register.
 - v. If FIRMWARE_OPS in progress bit is set, wait for FIRMWARE_OPS in progress bit to be clear for a maximum of FIRMWARE_OPS_TIMEOUT.
 - vi. If FIRMWARE_OPS in progress bit is not set, check FIRMWARE_OPS_STATUS register for status of generate firmware data region checksum. This operation shall never result in a failure from the module.
 - vii. Read FW_REGION_CRC0 and FW_REGION_CRC1 registers and verify the module calculated checksum matches the Host calculated checksum. If checksums do not match, Host may attempt to transfer the bytes again or abort the firmware update.
8. Commands the module to validate firmware image is valid for device based on common header.
 - a. Write NVDIMM_MGT_CMD1 register with value 0x2 (CL_FIRMWARE_OPS_STAT to 1) to clear the firmware ops status register.
 - b. Writes FIRMWARE_OPS_CMD register with value 0x10 (validate firmware image header) to ensure Host is transferring the correct image. The module shall validate that the common header transferred has the correct data. If it does not, module shall fail the FIRMWARE_OPS. If common header is valid, module shall persist at least the FIRMWARE IMAGE SIZE and FIRMWARE IMAGE CHECKSUM fields from the common header. These fields shall be used to determine whether a firmware image is valid or not.
 - c. Check for FIRMWARE_OPS in progress bit to be set in NVDIMM_CMD_STATUS0 register.
 - d. If FIRMWARE_OPS in progress bit is set, wait for FIRMWARE_OPS in progress bit to be clear for a maximum of FIRMWARE_OPS_TIMEOUT.
 - e. If FIRMWARE_OPS in progress bit is not set, check FIRMWARE_OPS_STATUS register for status of validate firmware image header. If FIRMWARE_OPS fails, abort the firmware update.
9. Commit the first firmware data region.
 - a. Clear the firmware ops status register. Write NVDIMM_MGT_CMD1 register with value 0x2 (CL_FIRMWARE_OPS_STAT to 1).
 - b. Write FIRMWARE_OPS_CMD register with value 0x8 (commit firmware data region).
 - c. Check for FIRMWARE_OPS in progress bit to be set in NVDIMM_CMD_STATUS0 register.
 - d. If FIRMWARE_OPS in progress bit is set, wait for FIRMWARE_OPS in progress bit to be clear for a maximum of FIRMWARE_OPS_TIMEOUT.
 - e. If FIRMWARE_OPS in progress bit is not set, check FIRMWARE_OPS_STATUS register for status of commit firmware data region. If this operation fails, Host may retry the operation or abort the firmware update.
10. Send and commit the rest of the firmware image data in REGION_BLOCK_SIZE sized regions. If the firmware image data size is not in increments of 32 bytes, Host shall pad the last block with zeroes so the transfer size is 32 bytes. For each firmware data region transfer, the Host does the following
 - a. Writes BLOCK_ID, REGION_ID0 and REGION_ID1 registers with the appropriate value starting at 0.
 - b. Clears the firmware data block to ensure there is no residual data.
 - i. Writes FIRMWARE_OPS_CMD register with value 0x2 (clear firmware data block).
 - ii. Check for FIRMWARE_OPS in progress bit to be set in NVDIMM_CMD_STATUS0 register.
 - iii. If FIRMWARE_OPS in progress bit is set, wait for FIRMWARE_OPS in progress bit to be clear for a maximum of FIRMWARE_OPS_TIMEOUT. If FIRMWARE_OPS in progress bit is not clear after FIRMWARE_OPS_TIMEOUT, abort the FIRMWARE_OPS command and abort firmware update.
 - iv. If FIRMWARE_OPS in progress bit is not set, check FIRMWARE_OPS_STATUS register for status of clear firmware data block. If not successful, abort the firmware update.

- c. Send the bytes from the first firmware data region to the module using either I²C block write to the TYPED_BLOCK_DATA_OFFSET register or I²C write byte to the TYPED_BLOCK_DATA_BYTES0 to TYPED_BLOCK_DATA_BYTES31. Data transfer will be done in 32 byte multiple. After a block has been transfer, increment and write the updated block identifier to the BLOCK_ID register and keep transferring blocks of data until all data in the region has been sent.
 - d. Assuming bytes were sent successfully, Host validates that the data was transferred correctly to the module by ensuring checksum calculated by module matches the Host for the firmware data region that has been transferred.
 - i. Calculates the checksum for the firmware data region transferred using the checksum algorithm described in Section B.1.15.1.
 - ii. Clear the firmware ops status register. Write NVDIMM_MGT_CMD1 register with value 0x2 (CL_FIRMWARE_OPS_STAT to 1).
 - iii. Commands the module to calculate checksum for the firmware data region. Write FIRMWARE_OPS_CMD register with value 0x4 (generate firmware data region checksum).
 - iv. Check for FIRMWARE_OPS in progress bit to be set in NVDIMM_CMD_STATUS0 register.
 - v. If FIRMWARE_OPS in progress bit is set, wait for FIRMWARE_OPS in progress bit to be clear for a maximum of FIRMWARE_OPS_TIMEOUT.
 - vi. If FIRMWARE_OPS in progress bit is not set, check FIRMWARE_OPS_STATUS register for status of generate firmware data region checksum. This operation shall never result in a failure from the module.
 - e. Read FW_REGION_CRC0 and FW_REGION_CRC1 registers and verify the module calculated checksum matches the Host calculated checksum. If checksums do not match, Host may attempt to transfer the bytes again or abort the firmware update.
 - f. Commit the firmware data region transferred.
 - i. Clear the firmware ops status register. Write NVDIMM_MGT_CMD1 register with value 0x2 (CL_FIRMWARE_OPS_STAT to 1).
 - ii. Write FIRMWARE_OPS_CMD register with value 0x8 (commit firmware data region).
 - iii. Check for FIRMWARE_OPS in progress bit to be set in NVDIMM_CMD_STATUS0 register.
 - iv. If FIRMWARE_OPS in progress bit is set, wait for FIRMWARE_OPS in progress bit to be clear for a maximum of FIRMWARE_OPS_TIMEOUT.
 - v. If FIRMWARE_OPS in progress bit is not set, check FIRMWARE_OPS_STATUS register for status of commit firmware data region. If this operation fails, Host may retry the operation or abort the firmware update.
11. After all of the firmware data has been transferred to the module, the Host shall ask the module to validate the firmware image data by the following
- a. Writes NVDIMM_MGT_CMD1 register with value 0x2 (CL_FIRMWARE_OPS_STAT to 1) to clear the firmware ops status register.
 - b. Writes FIRMWARE_OPS_CMD register with value 0x20 (validate firmware image) to command module to validate that a correct firmware image was committed. The module shall validate that the firmware image data size matches the FIRMWARE IMAGE SIZE value in the common header and the calculated checksum of the firmware image data matches the FIRMWARE IMAGE CHECKSUM value in the common header. The module may do additional checking to verify the firmware image committed is the correct image. If an incorrect image has been committed, module shall fail the FIRMWARE_OPS operation. If a correct image has been committed, module shall update SLOT1_FWREV0 and SLOT1_FWREV1 registers with the appropriate value.
 - c. Check for FIRMWARE_OPS in progress bit to be set in NVDIMM_CMD_STATUS0 register.
 - d. If FIRMWARE_OPS in progress bit is set, wait for FIRMWARE_OPS in progress to be clear for a maximum of FIRMWARE_OPS_TIMEOUT.
 - e. If FIRMWARE_OPS in progress bit is not set, check FIRMWARE_OPS_STATUS register for status of validate firmware image. If FIRMWARE_OPS fails, abort the firmware update.

12. The last step of a firmware update abort or when Host has completed the firmware update process is to disable firmware update mode on the module by the following
 - a. Writes NVDIMM_MGT_CMD1 register with value 0x2 (CL_FIRMWARE_OPS_STAT to 1) to clear the firmware ops status register.
 - b. Writes FIRMWARE_OPS_CMD register with the value 0x0 to disable firmware update mode.
 - c. Check for FIRMWARE_OPS in progress bit to be set in NVDIMM_CMD_STATUS0 register.
 - d. If FIRMWARE_OPS in progress bit is set, wait for FIRMWARE_OPS in progress bit to be clear for a maximum of FIRMWARE_OPS_TIMEOUT.
 - e. If FIRMWARE_OPS in progress bit is not set, check FIRMWARE_OPS_STATUS register for status of disable firmware update mode.

To select which firmware image to run, Host writes to the SELECTED_FW_SLOT field in the FW_SLOT_INFO register with either 0 or 1. On the next power cycle or controller reset, the module shall use the firmware image from the selected slot. If the selected does not have a valid image, module shall revert to the firmware image from slot 0.

If a Firmware Operation fails, the Host may retrieve information about the cause of the failure by reading the Vendor Log Page.

B.3.6 Typed Block Data Workflow

This section describes the recommended workflow for a Host to read and write to a Typed Block Data. If the module supports Operational Unit Buffer Per Typed Block Data, the Host can do transfers to multiple Typed Block Data in parallel. If the module does not support Operational Unit Buffer Per Typed Block Data, the Host should do transfers to a Typed Block Data at a time.

The Operational Unit operations may time out. The Host shall use the OPERATIONAL_UNIT_OPS_TIMEOUT0 and OPERATIONAL_UNIT_OPS_TIMEOUT1 registers to determine the maximum amount of time to wait for an Operational Unit operation to complete.

B.3.6.1 Reading Typed Block Data

To read from a Typed Block Data, the Host shall do the following:

1. Determine the number of blocks to read for the Typed Block Data and calculate the starting Operational Unit ID for the desired data.
2. Set TYPED_BLOCK_DATA to the desired Typed Block Data value.
3. Set Bit 2, Clear Operational Unit Buffer, to 1 in the OPERATIONAL_UNIT_OPS_CMD register to clear the intermediate buffer on the module. Poll the OPERATIONAL_UNIT_OPS_STATUS register for completion of Clear Operational Unit Buffer command.
4. Set OPERATIONAL_UNIT_ID0 and OPERATIONAL_UNIT_ID1 to the Operational Unit ID of the desired data.
5. Set Bit 0, Get Operational Unit, to 1 in the OPERATIONAL_UNIT_OPS_CMD register to retrieve the data into an intermediate buffer on module. Poll the OPERATIONAL_UNIT_OPS_STATUS register for completion of Get Operational Unit command.
6. Set Bit 3, Generate Operational Unit CRC, to 1 in the OPERATIONAL_UNIT_OPS_CMD register to request the module to calculate the Operational Unit CRC value for the data retrieved.
7. Set the BLOCK_ID, REGION_ID0 and REGION_ID1 registers to the appropriate value within the Operational Unit.
8. Read either TYPED_BLOCK_DATA0 to TYPED_BLOCK_DATA31 registers or the TYPED_BLOCK_DATA register to read the data for the block from the module.
9. Increment the BLOCK_ID register. If the BLOCK_ID register has the value 255, set the BLOCK_ID register to 0 and increment the REGION_ID0 and REGION_ID1 registers.
10. Repeat Steps 8 to 9 until all the data from the Operational Unit is retrieved.

11. To ensure there is no data error during transfer of the Operational Unit data, the Host should calculate the CRC for Operational Unit data received from the module and verify that the CRC value matches the values in the OPERATIONAL_UNIT_CRC0 and OPERATIONAL_UNIT_CRC1 registers.
12. Increment Operational Unit ID in the OPERATIONAL_UNIT_ID0 and OPERATIONAL_UNIT_ID1 registers.
13. Repeat Steps 3 to 12 until all desired data is retrieved.

B.3.6.2 Writing Typed Block Data

To write to a Typed Block Data, the Host shall do the following:

1. Determine the number of blocks to write for the Typed Block Data and calculate the starting Operational Unit ID of the data to be written.
2. Set TYPED_BLOCK_DATA to the desired Typed Block Data value.
3. Set Bit 2, Clear Operational Unit Buffer, to 1 in the OPERATIONAL_UNIT_OPS_CMD register to clear the intermediate buffer on the module. Poll the OPERATIONAL_UNIT_OPS_STATUS register for completion of Clear Operational Unit Buffer command.
4. Set the OPERATIONAL_UNIT_ID0 and OPERATIONAL_UNIT_ID1 registers to the Operational Unit ID of the data to be written.
5. Calculate the Operational Unit CRC for the Operational Unit data to be written.
6. Set the BLOCK_ID, REGION_ID0 and REGION_ID1 registers to 0.
7. Write data to either TYPED_BLOCK_DATA0 to TYPED_BLOCK_DATA31 registers or the TYPED_BLOCK_DATA register to send data to the module.
8. Increment the BLOCK_ID register. If the BLOCK_ID register has the value 255, set the BLOCK_ID register to 0 and increment the REGION_ID0 and REGION_ID1 registers.
9. Repeat Steps 7 to 8 until all the data from the Operational Unit is sent.
10. Set Bit 3, Generate Operational Unit CRC, to 1 in the OPERATIONAL_UNIT_OPS_CMD register to request the module to calculate the Operational Unit CRC value for the data retrieved.
11. To ensure there is no data error during transfer of the Operational Unit data, the Host shall verify that the CRC value calculated in step 5 matches the values in the OPERATIONAL_UNIT_CRC0 and OPERATIONAL_UNIT_CRC1 registers.
12. Set Bit 1, Set Operational Unit, to 1 in the OPERATIONAL_UNIT_OPS_CMD register to commit the Operational Unit data on the module. Poll the OPERATIONAL_UNIT_OPS_STATUS register for completion of Get Operational Unit command.
13. Increment the Operational Unit ID in the OPERATIONAL_UNIT_ID0 and OPERATIONAL_UNIT_ID1 registers.
14. Repeat Steps 3 to 13 until all desired data is retrieved.

Typed Block Data updates shall be supported only at Operational Unit size granularity. If the Host is updating data that does not start at the beginning of an Operational Unit or the last byte is not at the end of an Operational Unit, the Host needs to first read in the Operational Unit data before modifying it.

Annex C (informative) Differences between revisions

This annex briefly describes most of the differences between the text of this standard, JESD304-4.01, and its predecessor JESD304-4 (November 2020). Some minor formatting and/or punctuation changes may have been made however they are not indicated in this annex.

Clause	Description of Change
4.5	Second paragraph stated “Table 3” corrected to “Table 109”.
Annex B	This Annex was incorrectly left out of the original publication (JCB-20-25).



Standard Improvement Form

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